Simulators

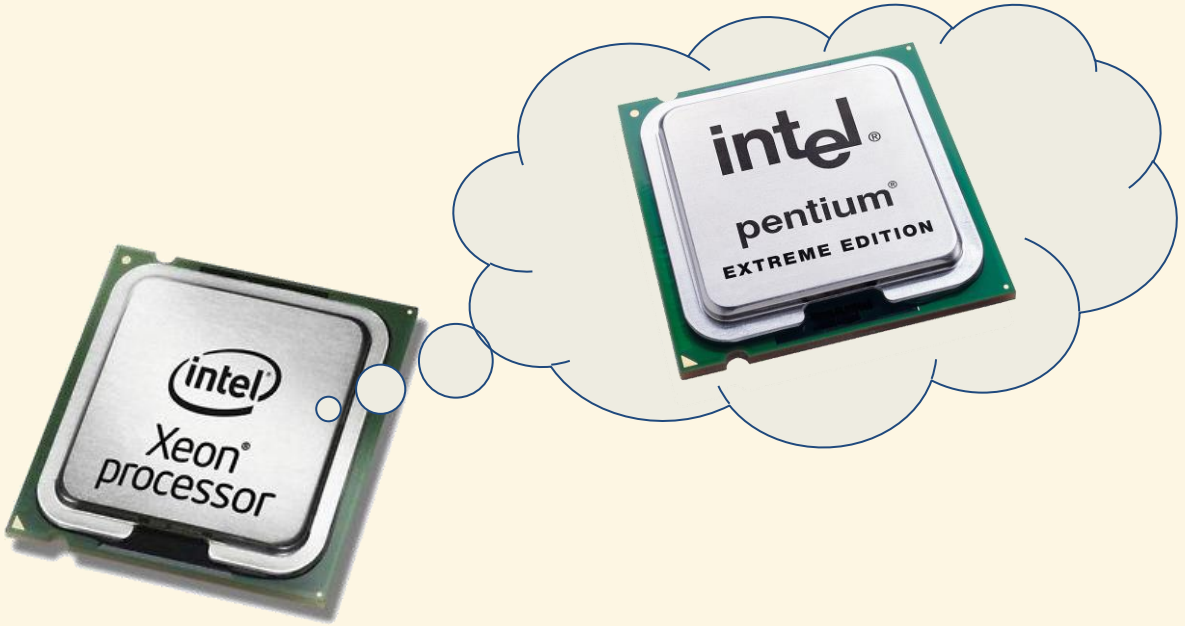
5SIA0

Patrick Wijnings

(Original slides by Luc Waaijen)

Processors Processing Processors

The meta-lecture



Why Simulators?

Your Friend Harm

Why Simulators?

Harm Loves Tractors

Harm

Why Simulators?

Unfortunately for Harm you need to go outside to drive tractors

Harm

The outside world

Why Simulators?

And the outside world is filled with dangers

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Scary Animals!

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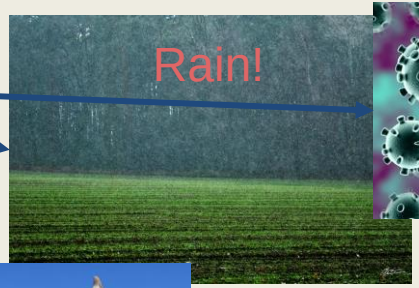
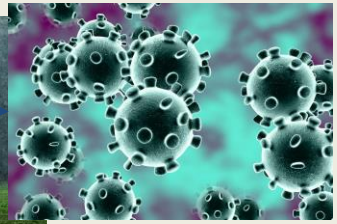


Rain!



Virusses!

Scary Animals!

Why Simulators?

Harm

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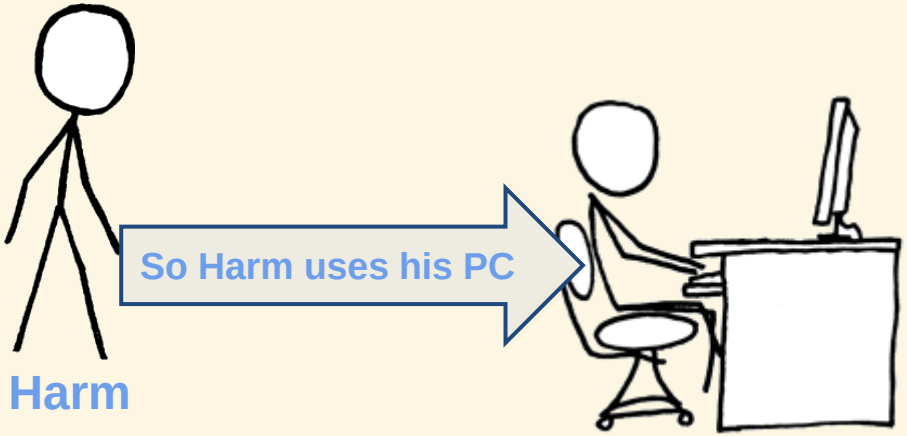

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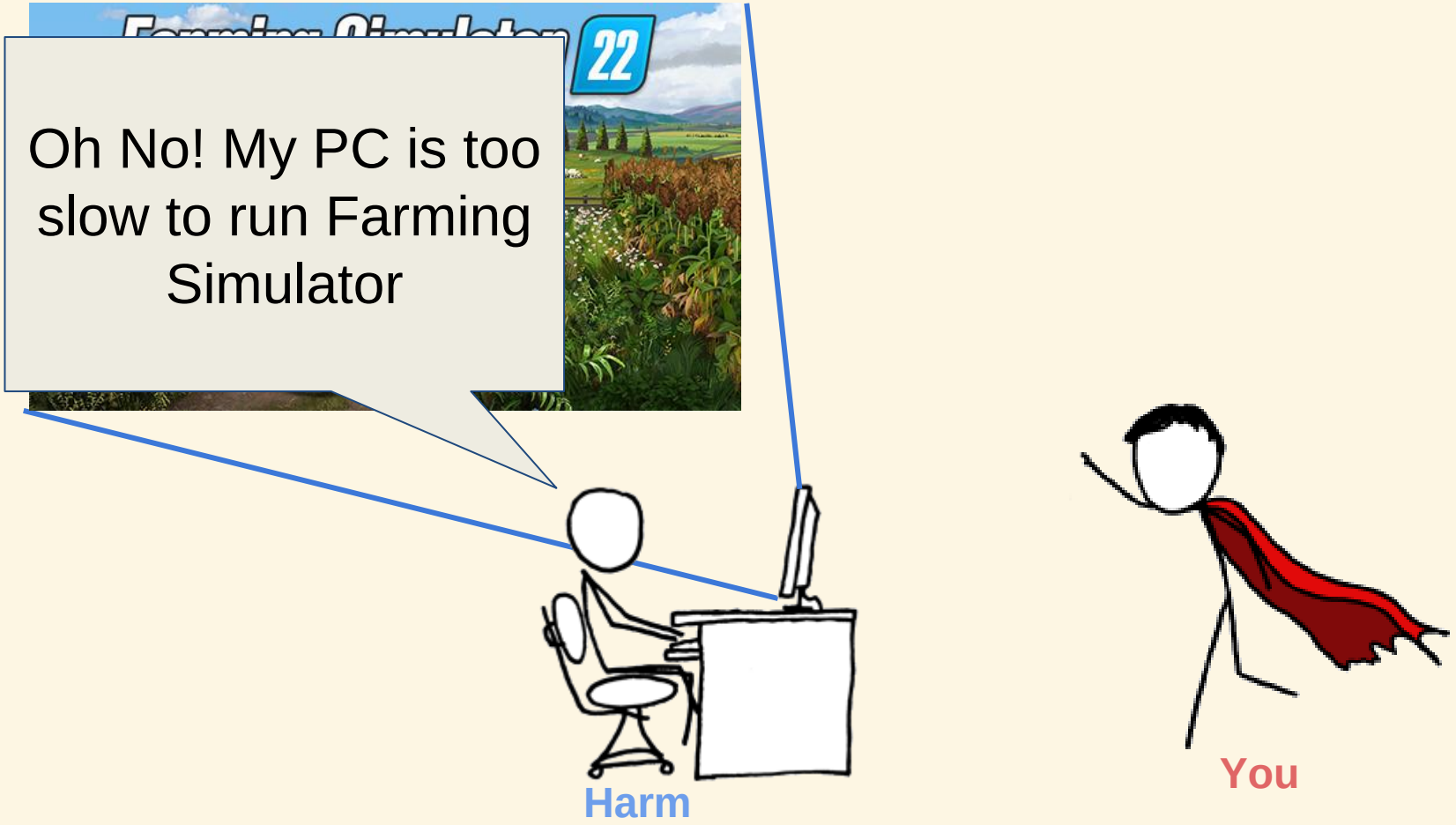

Why Simulators?

Oh No! My PC is too slow to run Farming Simulator

Harm

Stand back!
I'm a **computer architect**!

You

How to help Harm?

Of course you have many ideas on how to speed-up Harms computer.

But which ones should you apply?

You

Design Space Exploration Options

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Buy (or build) all hardware options

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Use analytical models

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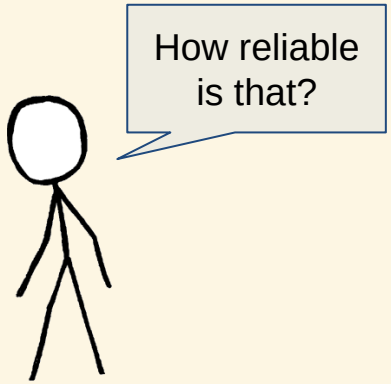

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Simulate the design points!

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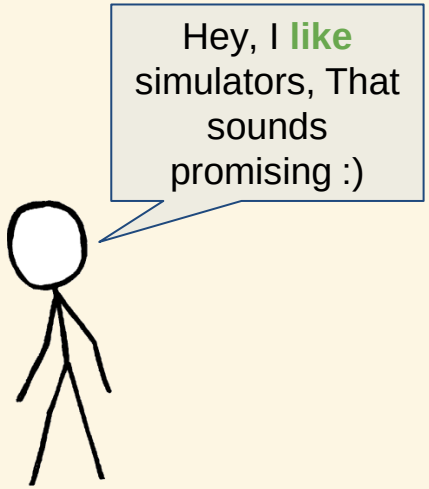

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- Performance
- Energy
- Power (**!=Energy**)
- Thermal

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Cycle accurate vs Functionality
Caches
Full operating system
Disk accesses
Background tasks
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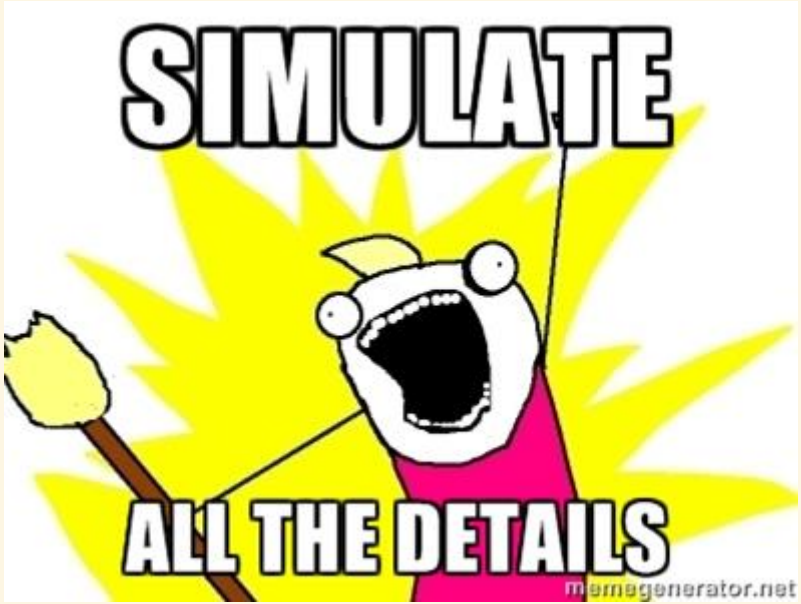
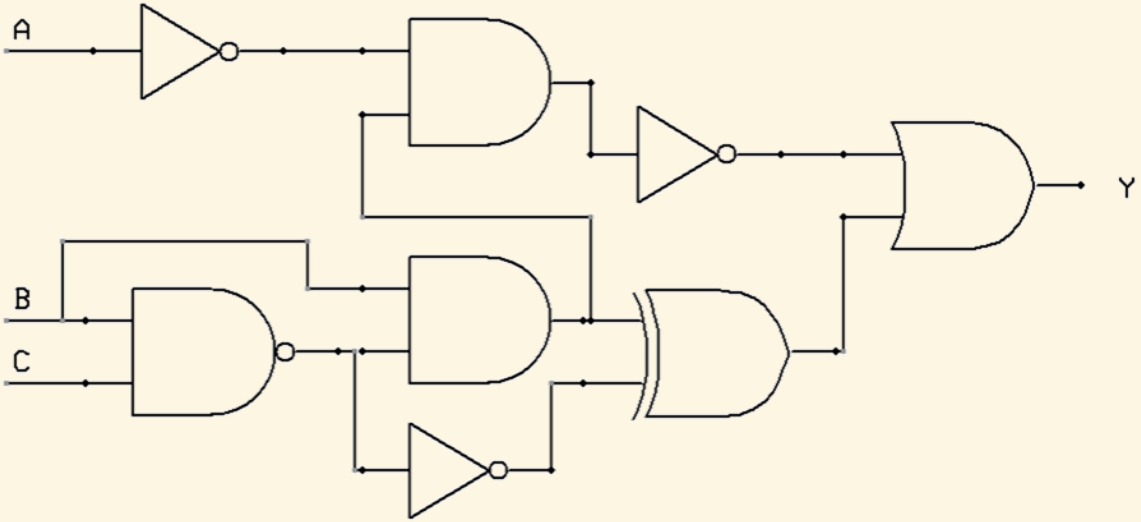


All the details: RTL Simulation

All the details: RTL Simulation

Simulate at **gate level**:



All the details: RTL Simulation

Simulate at **gate level**:

- modelsim/questasim (Mentor)
- ncsim (Cadence)
- VCS (Synopsys)
- Icarus Verilog (Open Source!)
- ...

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- Highest level of precision and detail

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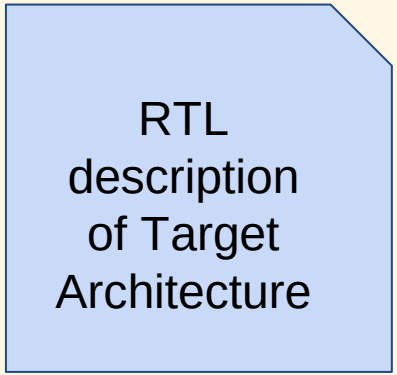
Nvidia GPU with > 1 Billion transistors
Small tests take over 8 hours! [1]

[1] http://www.deepchip.com/items/0523-04.html

modified from http://xkcd.com/303/

Slightly less horribly slow: Hardware Emulation



Slightly less horribly slow: Hardware Emulation

RTL description of Target Architecture

Synthesize for FPGA (slow)

Slightly less horribly slow: Hardware Emulation

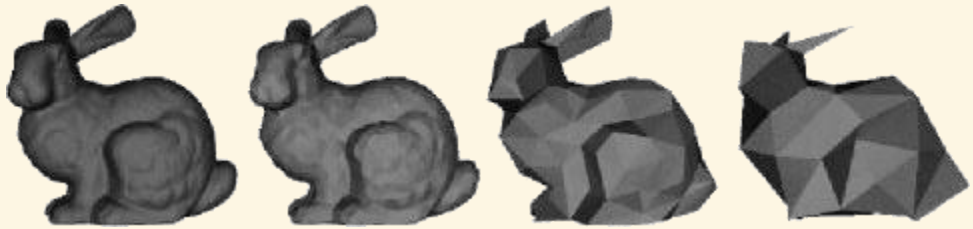
RTL description of Target Architecture

Synthesize for FPGA (slow)

Emulate on FPGA (fast!)
Note: instrumentation required to get detailed information out!

Levels of detail in Simulation

- Full-System versus User-level
- Cycle Accurate versus Functional
- Execution- versus Trace-driven



To OS or not to OS?

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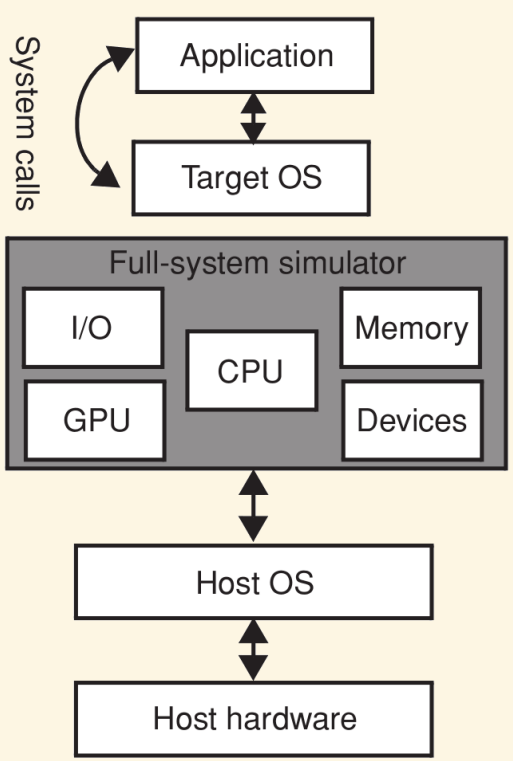

Full-System

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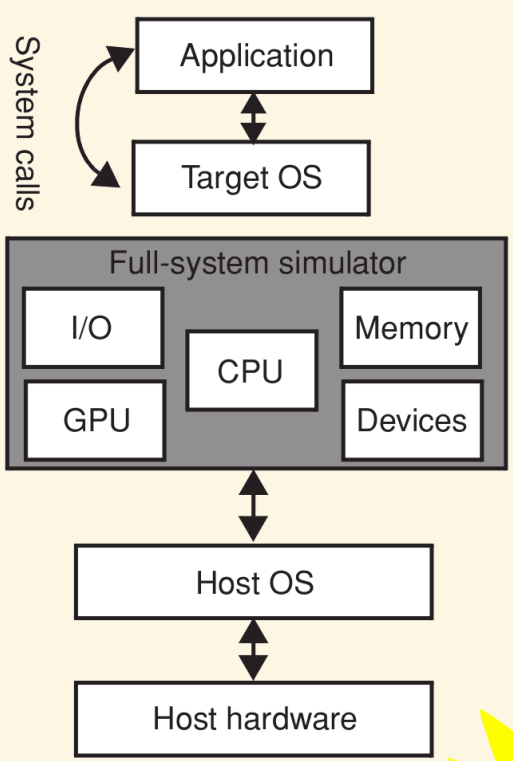

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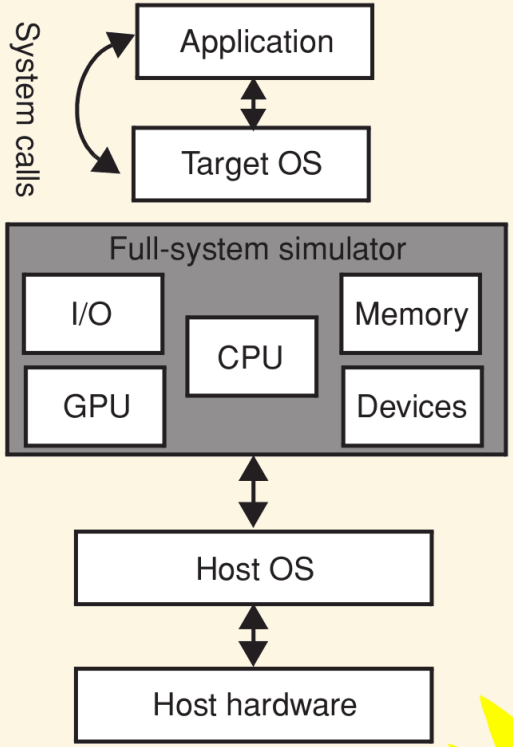

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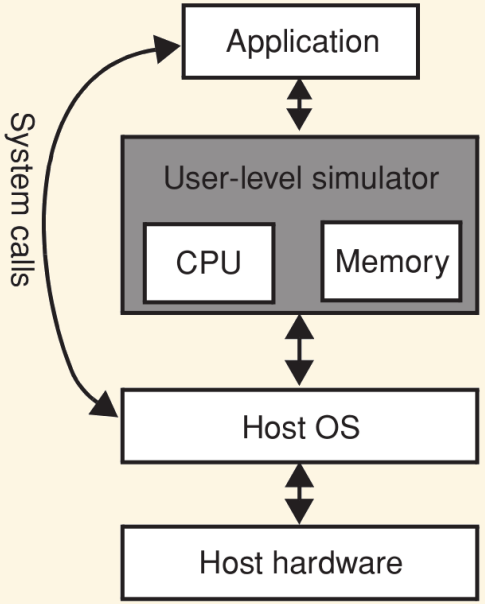

User-Level

User-Level

Famous example: **Simple Scalar [1]**

Advantages

- Fast to develop and update to new architectures
- Usually ‘accurate enough’

Disadvantages

- Any time spent in the OS is not modelled accurately. Can have severe impact, database applications spent 20-30% of their time in OS mode.

[1] http://www.simplescalar.com/

Cycle Accurate versus Functional

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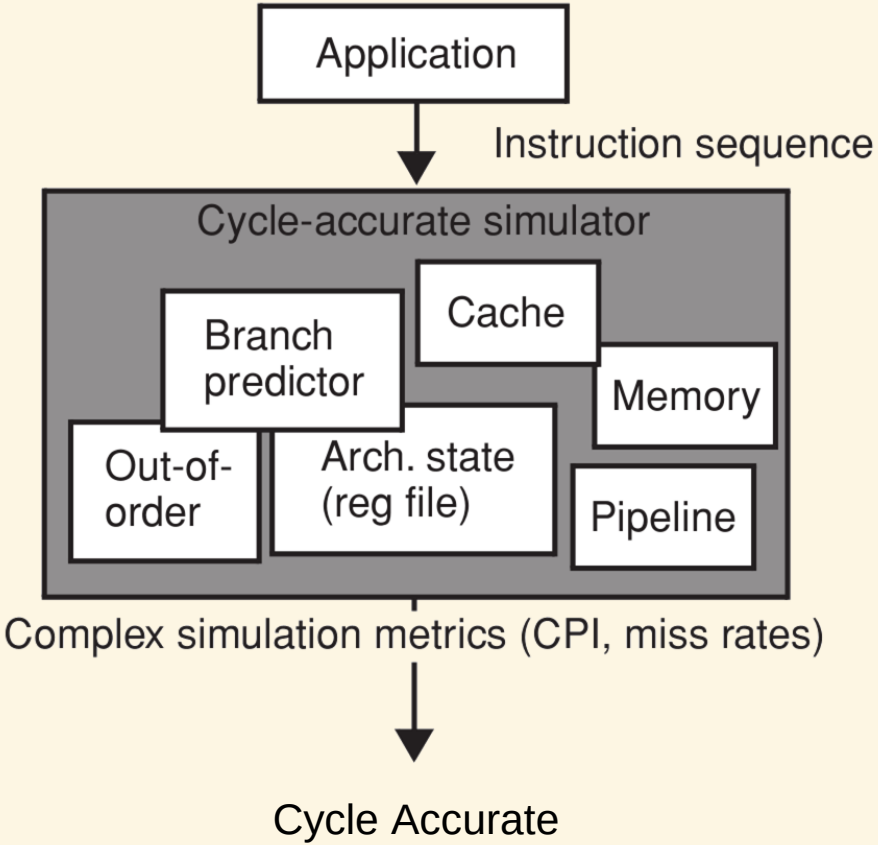

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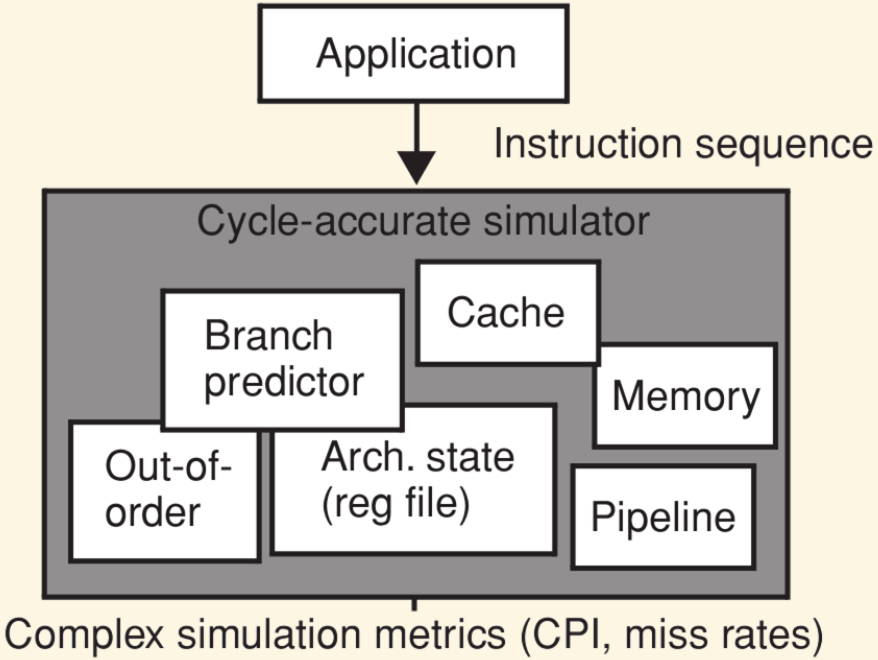

Cycle Accurate

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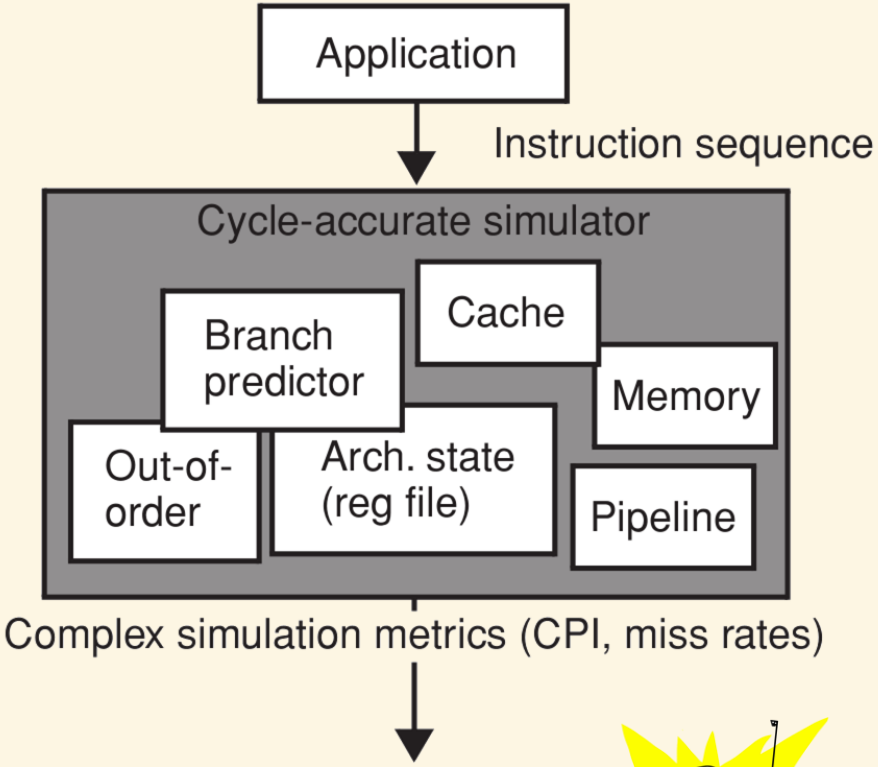
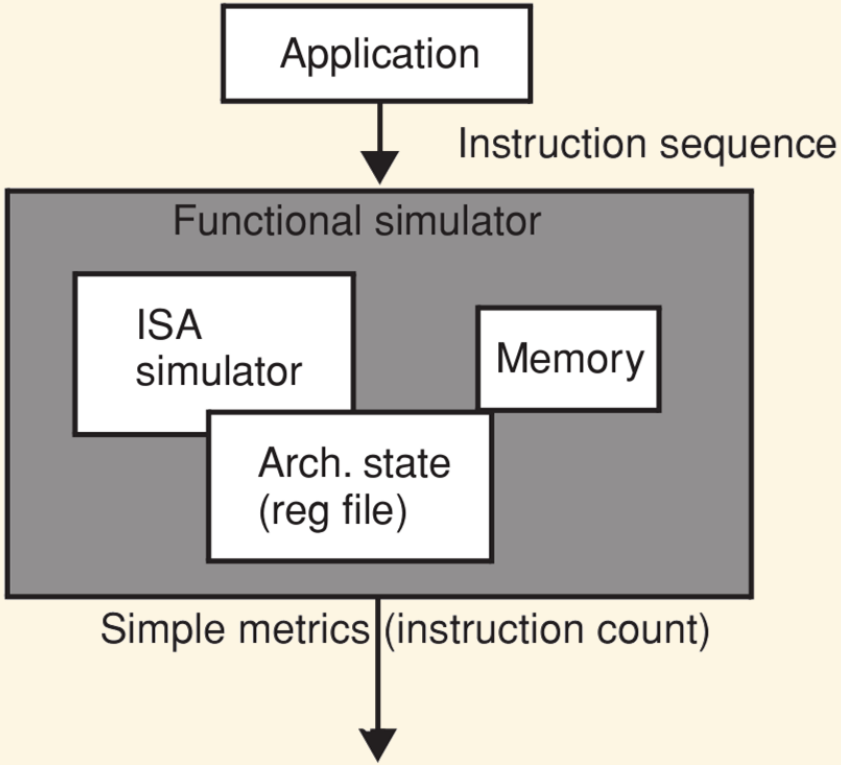




Cycle Accurate versus Functional

Functional - no/limited model of the micro architecture

An (add) instruction of the target can be translated to an (add) instruction on the host, and be simulated that way.

Example 1: Simple Scalar sim-fast

Example 2: QEMU, Full-system emulator using dynamic translation

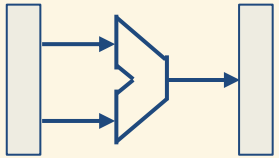
Cycle Accurate - includes model of the micro architecture

Block resources in the pipeline when instruction executes

Use target branch predictor scheme

Out-of-order execution

Example: Simple Scalar sim-outorder



Execution- versus Trace-driven

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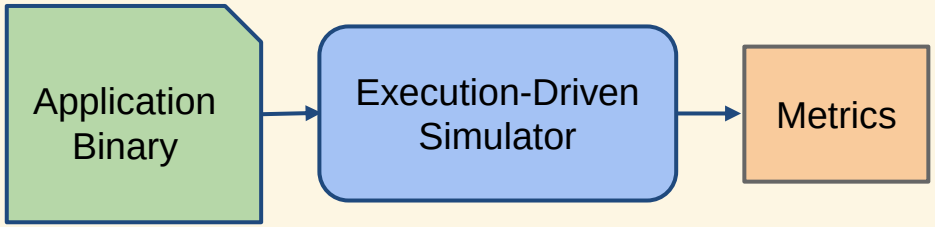

Execution Driven: application executes on simulator

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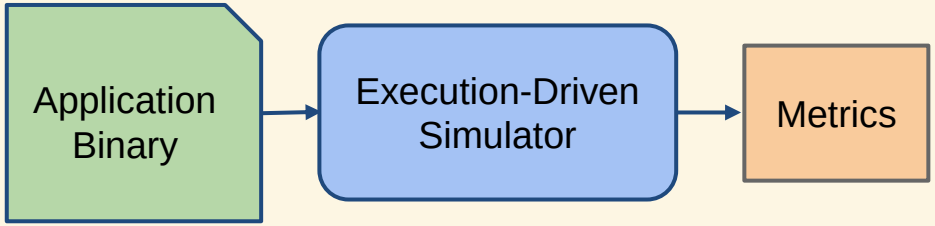

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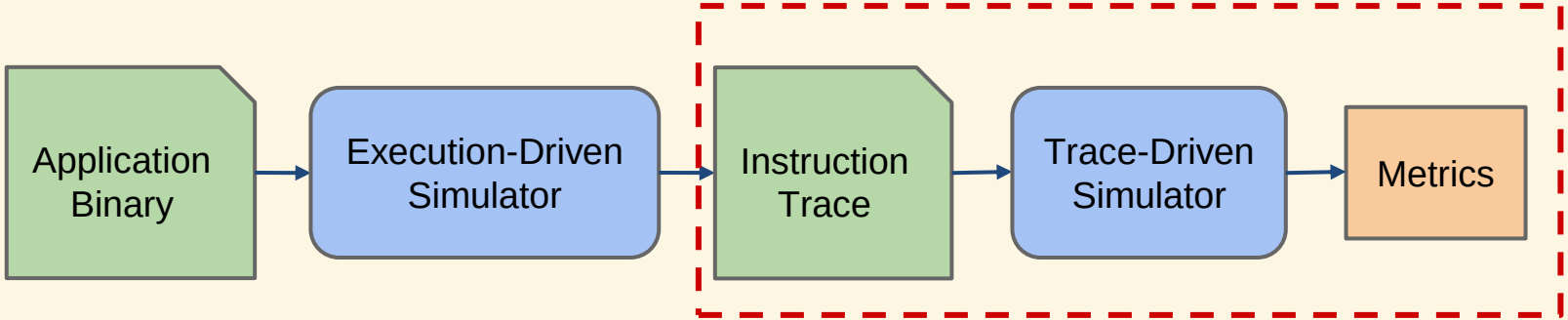
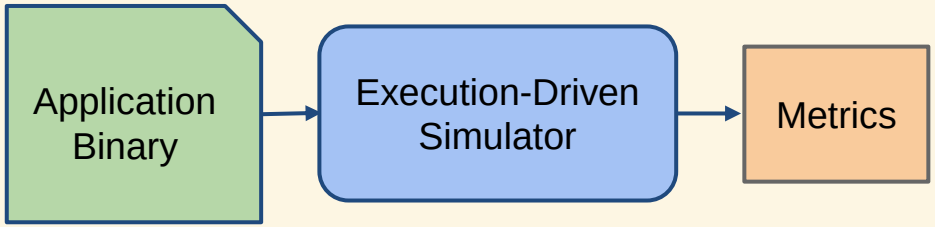


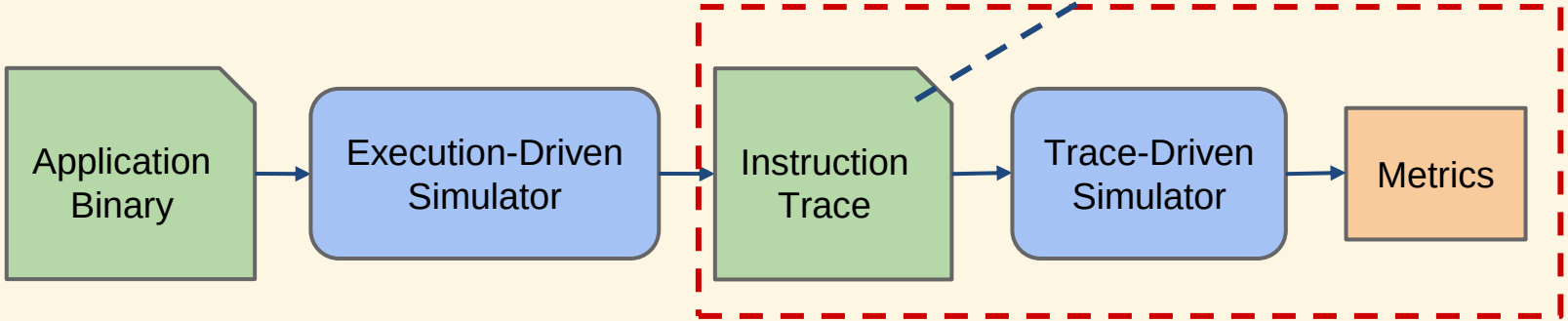
Trace Driven: simulator uses trace as input

Execution- versus Trace-driven



Execution Driven: application executes on simulator

```
mov edx,len
mov ecx,msg
mov ebx,1
mov eax,4
int 0x80
```



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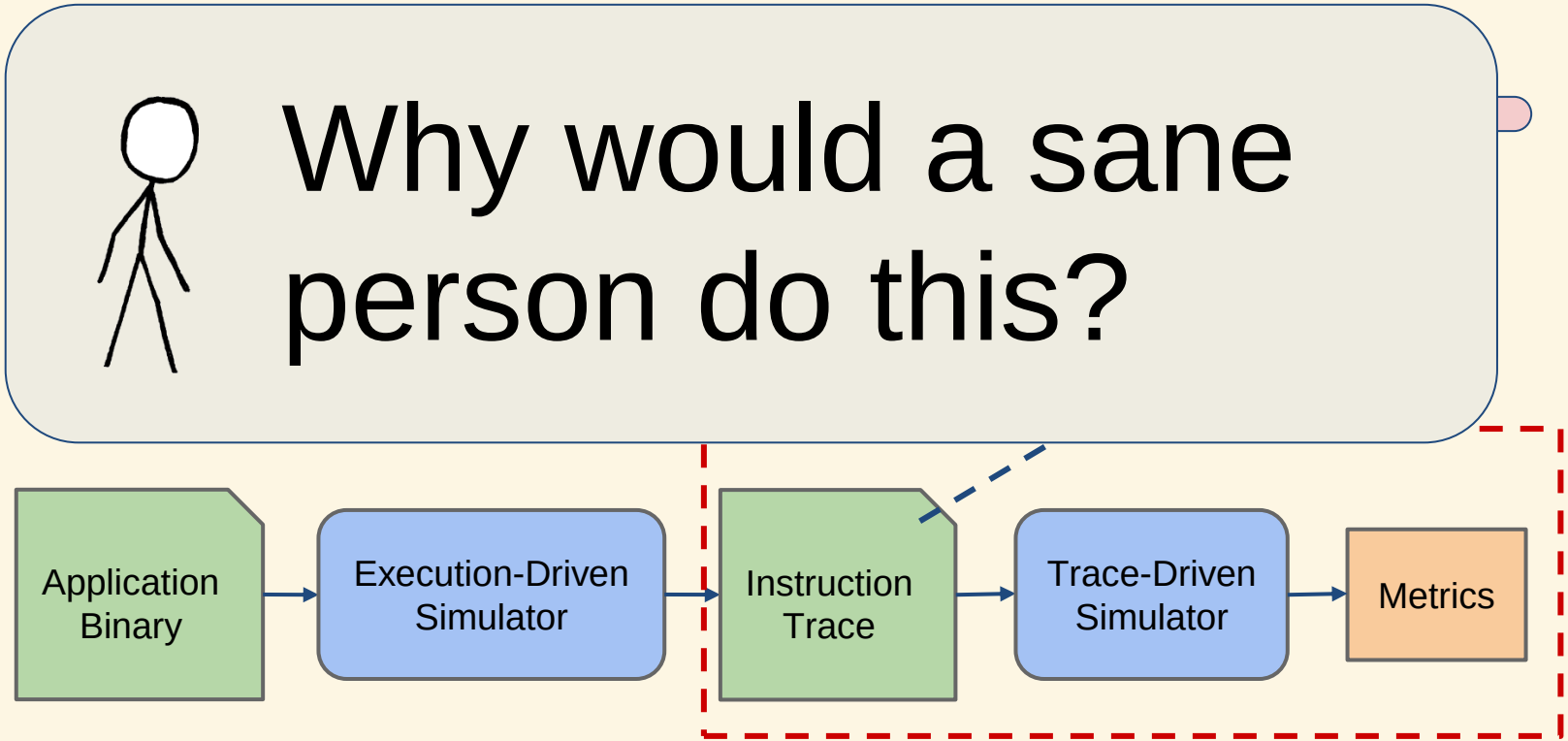

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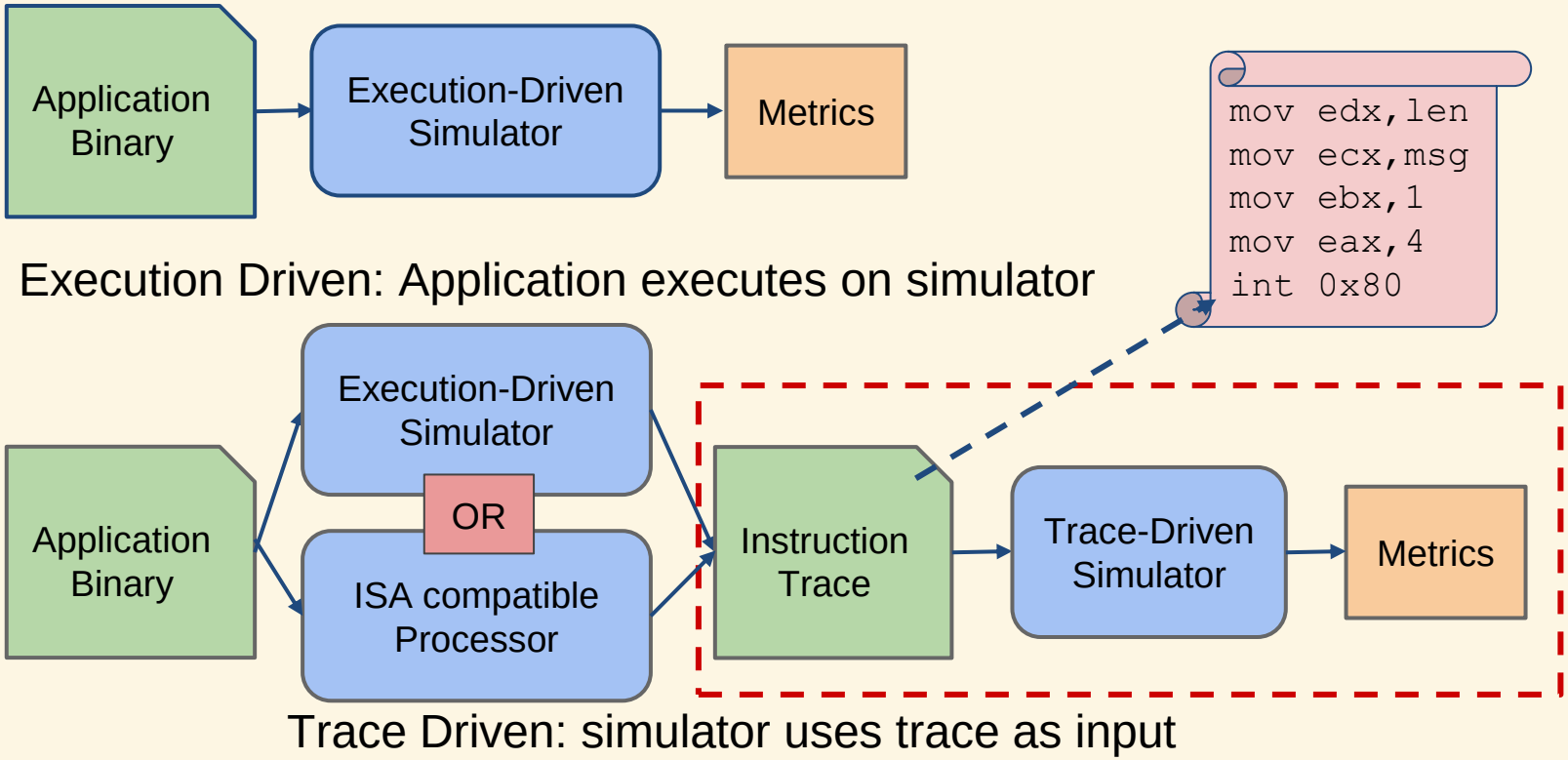

Trace-driven Simulation

Advantages

- Trace collection only required once
- Trace collection can be done with ISA compatible processor
- Trace simulator does not need to simulate all instructions, can skip ahead in trace if not implemented

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Disadvantages

- Cannot speculatively execute code (trace is fixed)
- Trace file can become huge for large applications (hundreds of GBs)

Mixing Simulation Strategies

Direct-execution

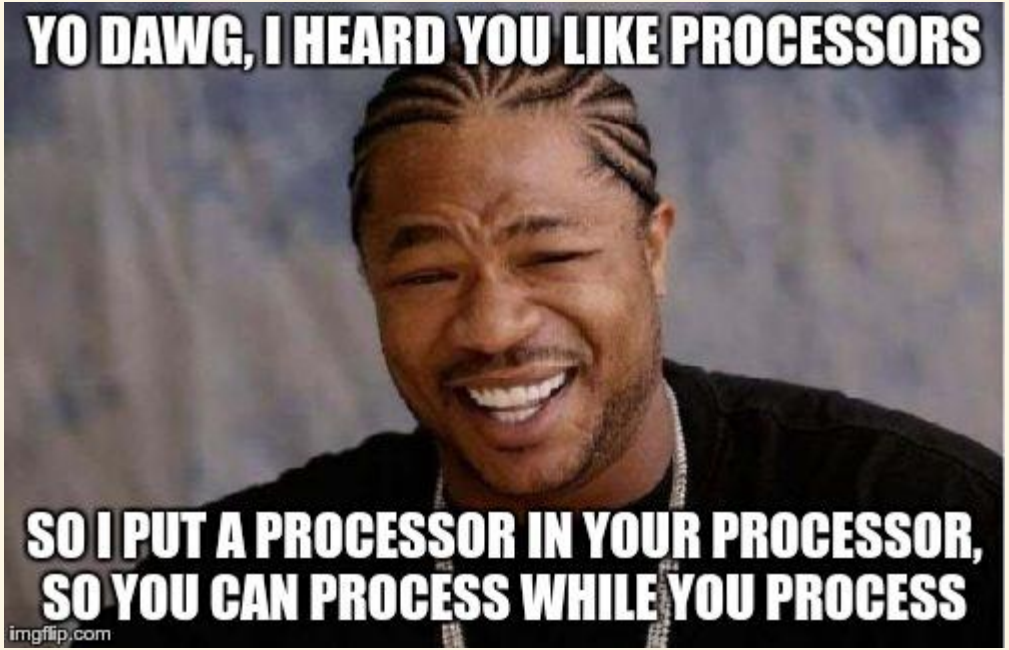
Parts execute directly on the host (e.g. using dynamic translation such as QEMU)

Other parts are executed on cycle accurate simulation

Use case:

Interested in memory accesses and memory behavior. Execute only loads and stores on the simulator, emulate the rest directly on the host machine

Simulation in the Multiprocessor Era



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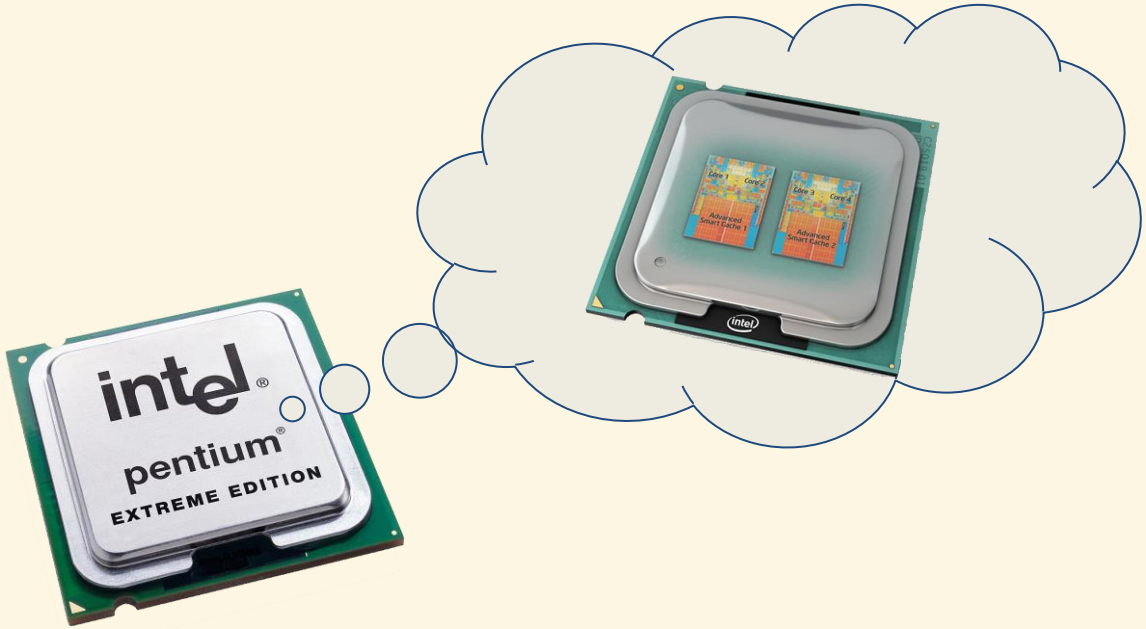
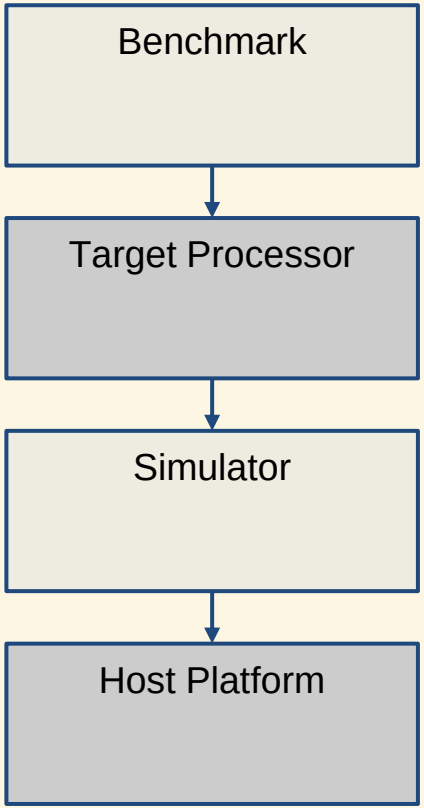


Parallelisation in all levels of the simulation stack



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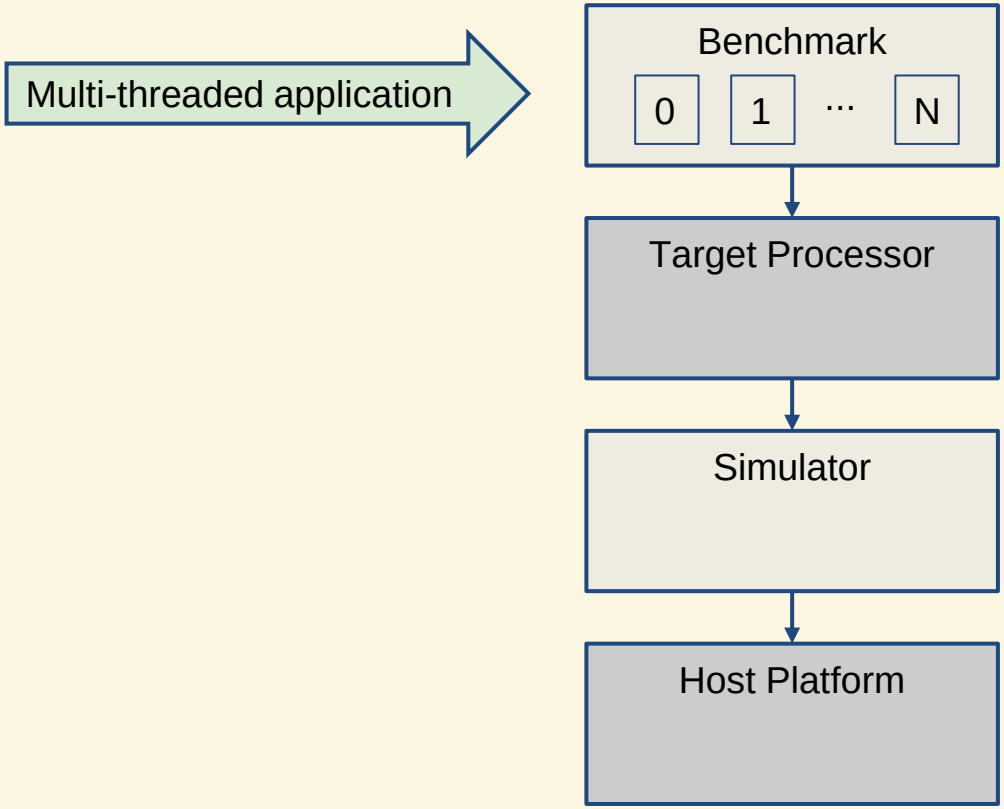

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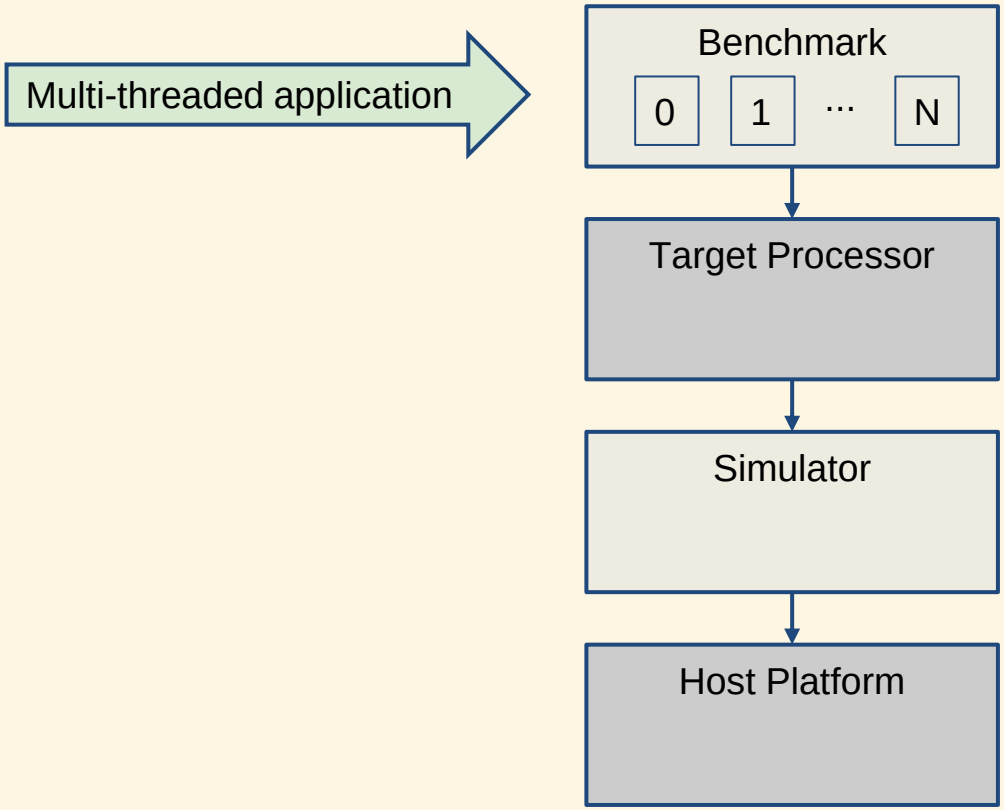

A multi-threaded application running on a single core target processor.

Question: Does this make sense?

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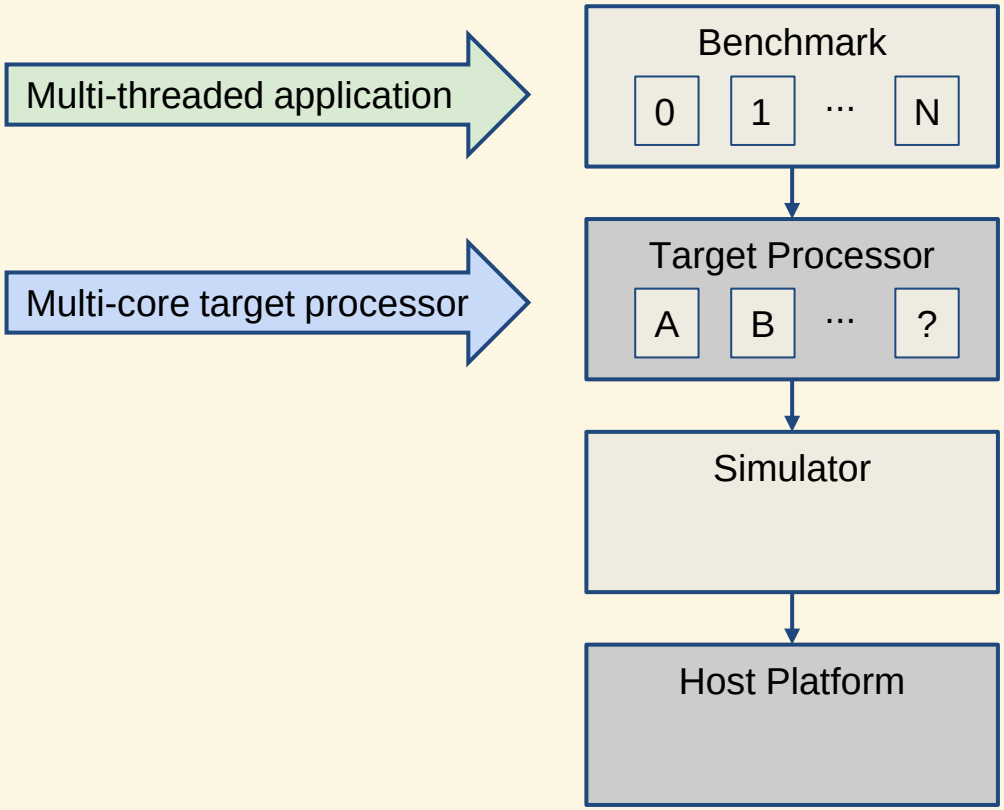

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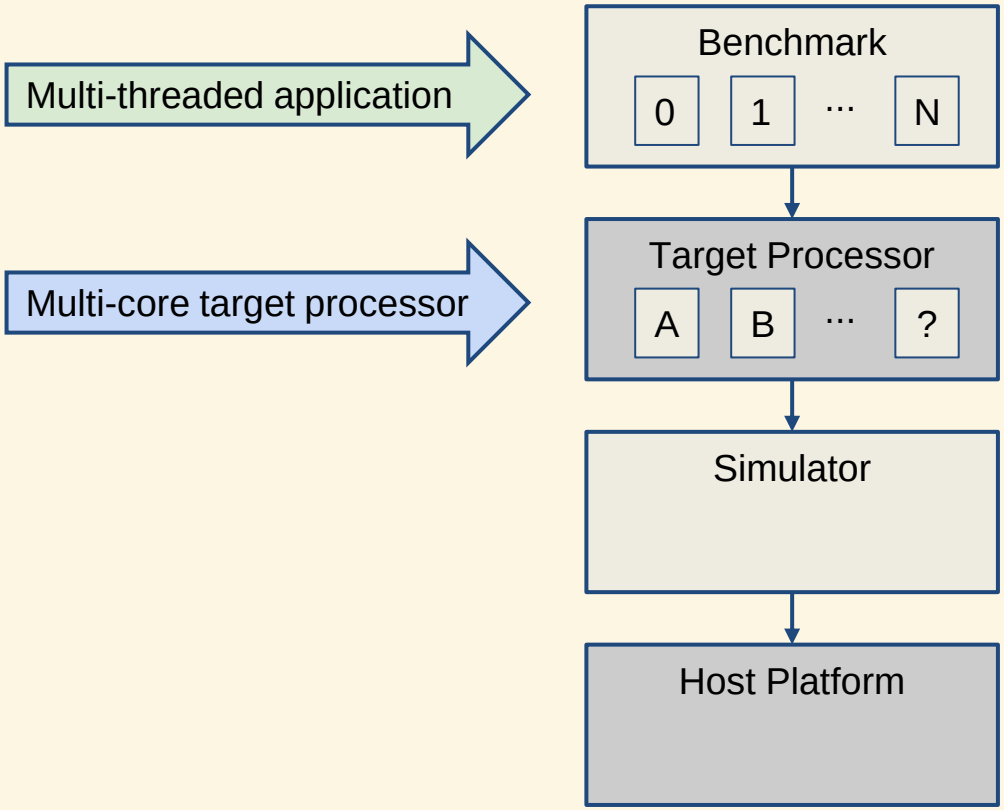

A multi-core processor running on a single threaded simulator.

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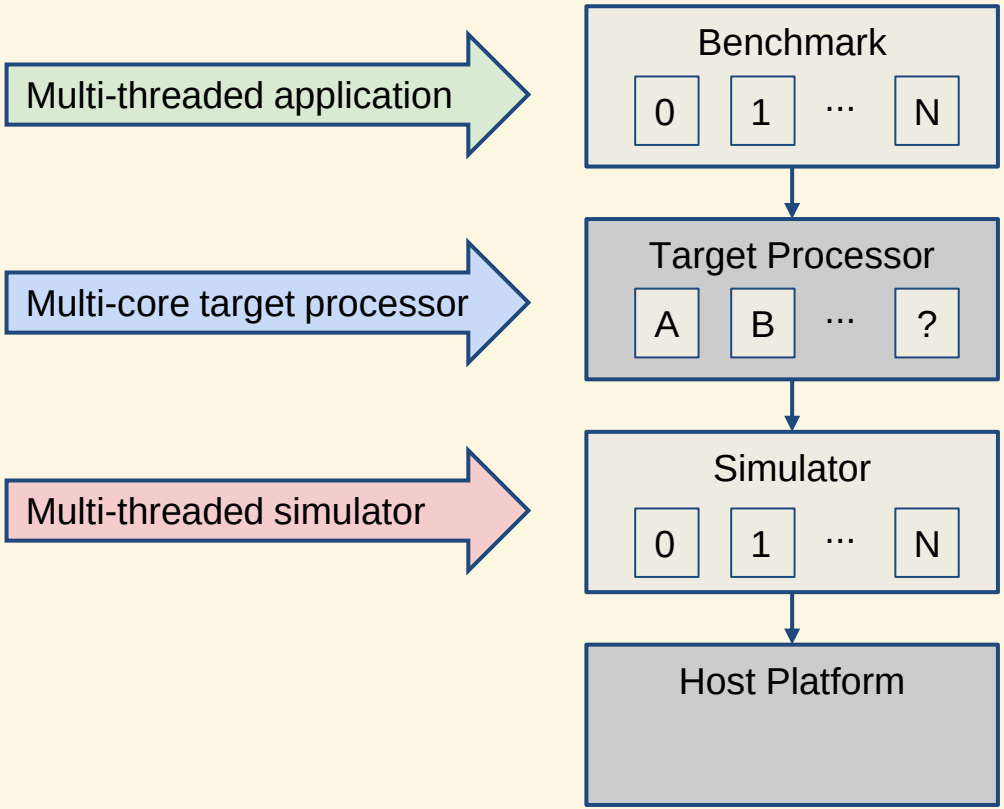

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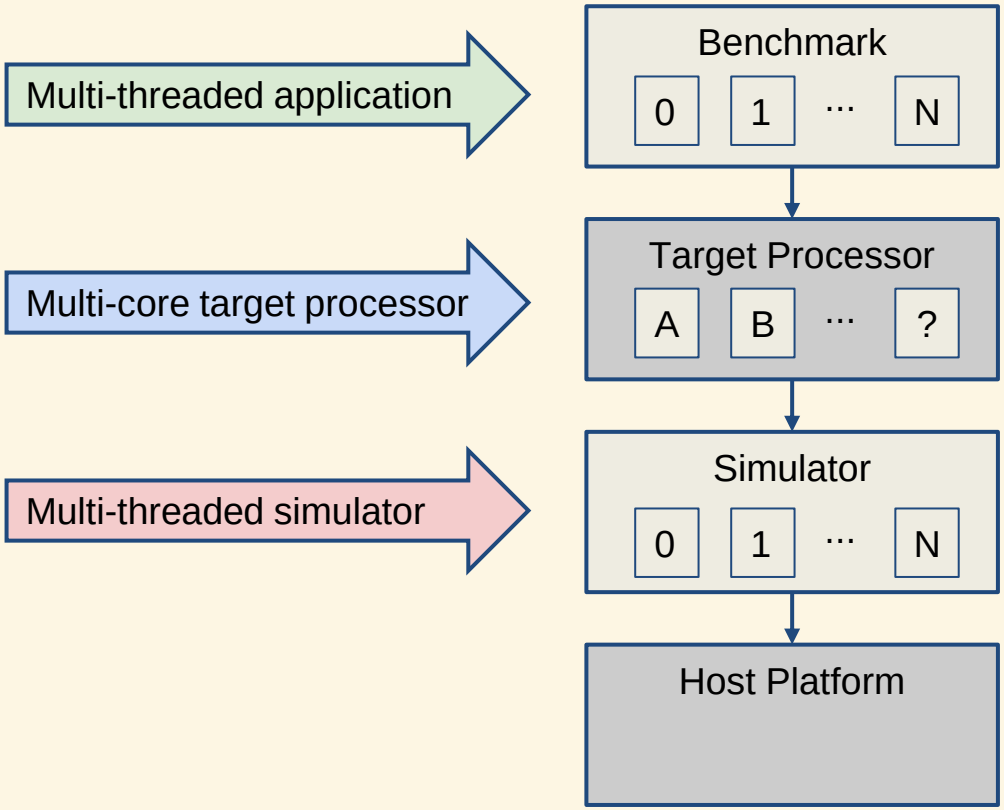

A multi-threaded simulator running on a single-core host.

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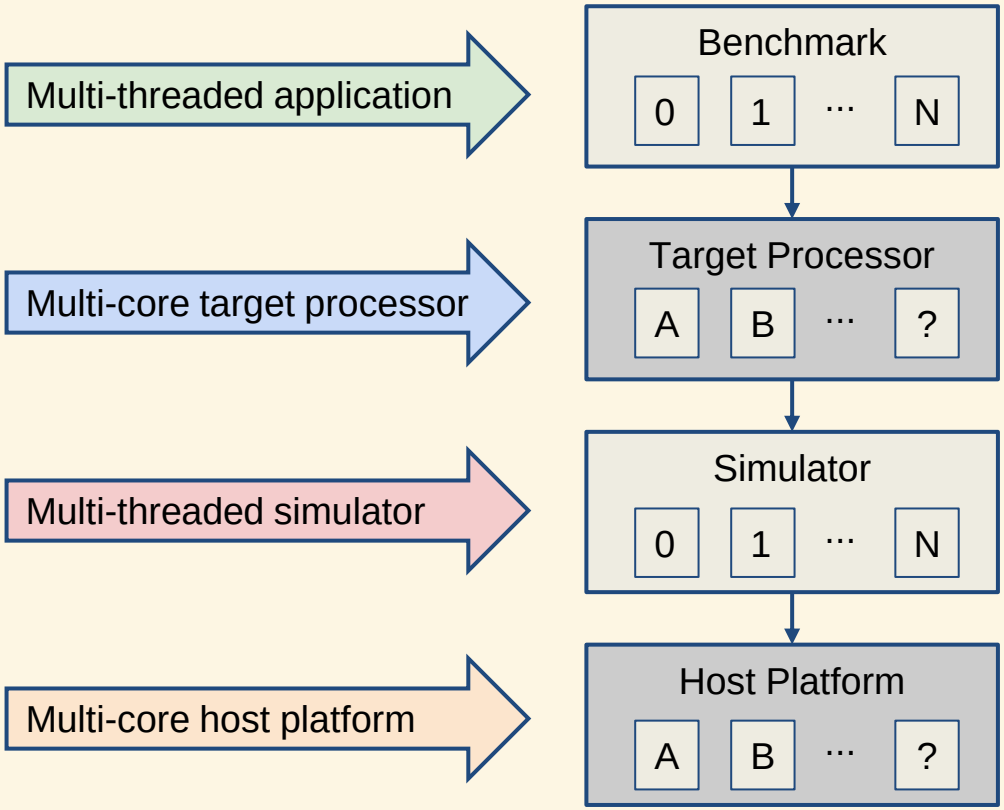

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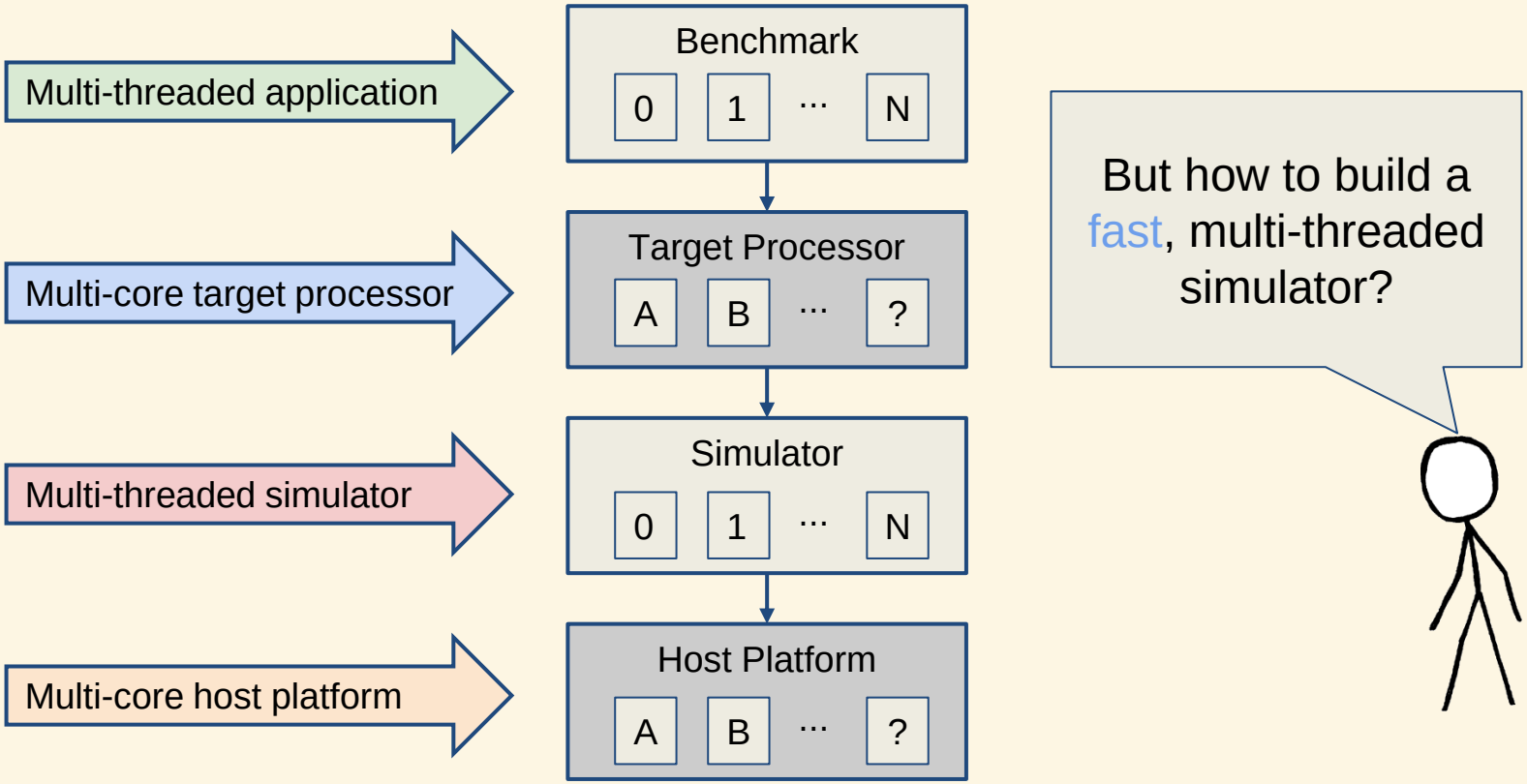
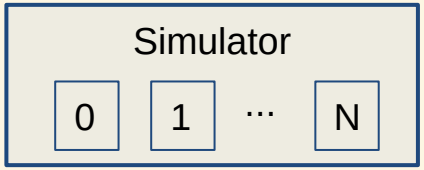
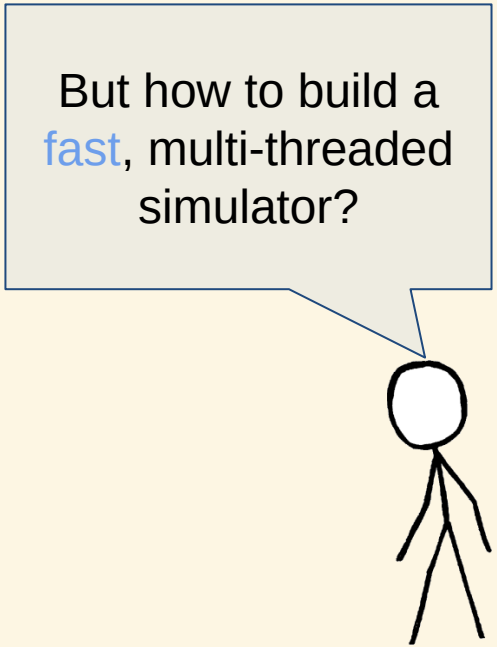


Parallelisation in all levels of the simulation stack

Multi-threaded simulator





Parallel Simulation Techniques

- Discrete event simulation
- Quantum simulation
- Slack simulation

Parallel Simulation Techniques

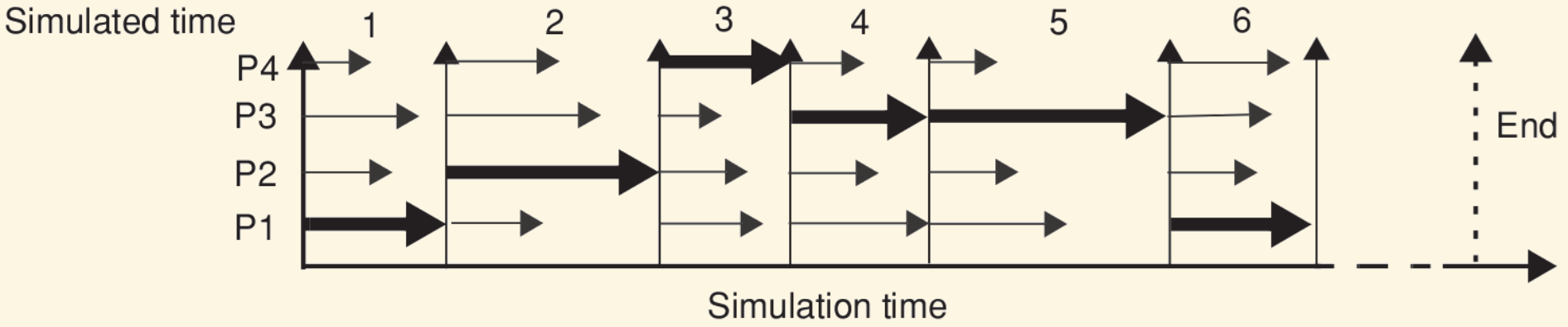
Discrete event simulation

Quantum simulation

Slack simulation

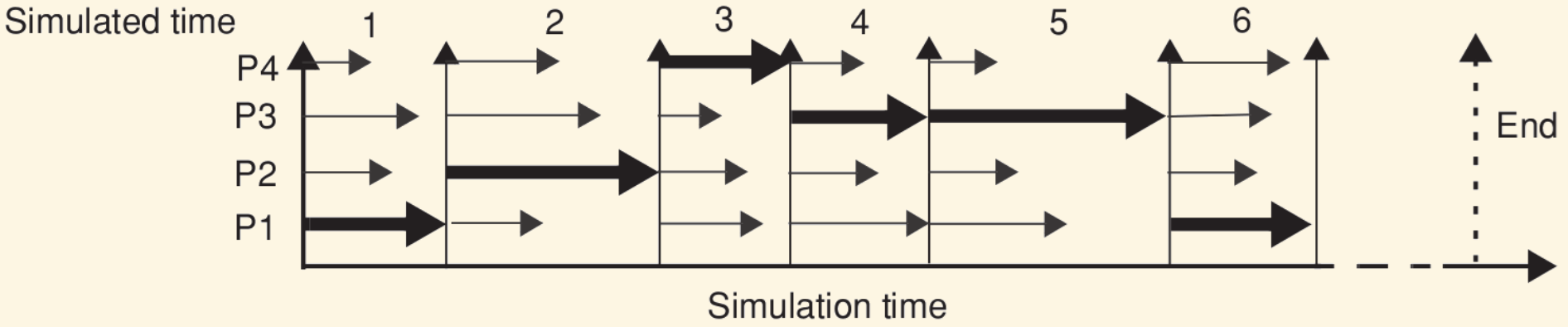
Not schrödinger's cat
‘quantum’ though

Discrete-Event Simulation



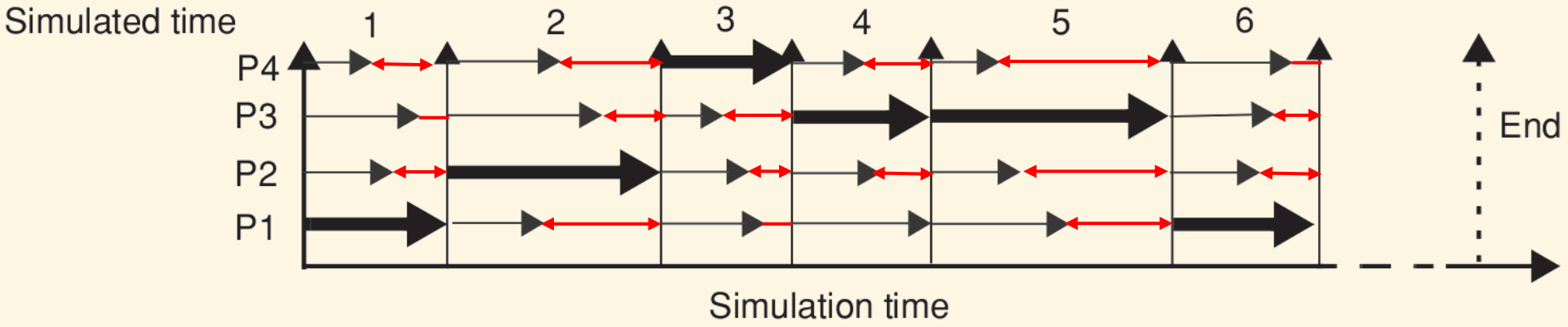
A logical choice for a simulator “time step” is one cycle for the fastest core.

Discrete-Event Simulation



Disadvantage

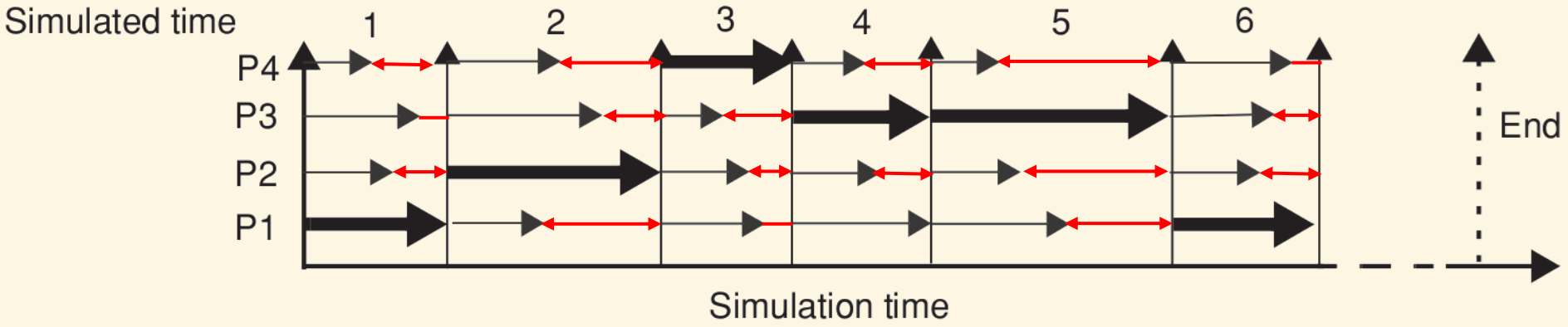
Discrete-Event Simulation



Disadvantage

Under utilisation of the host platform if threads are idle for synchronisation

Discrete-Event Simulation



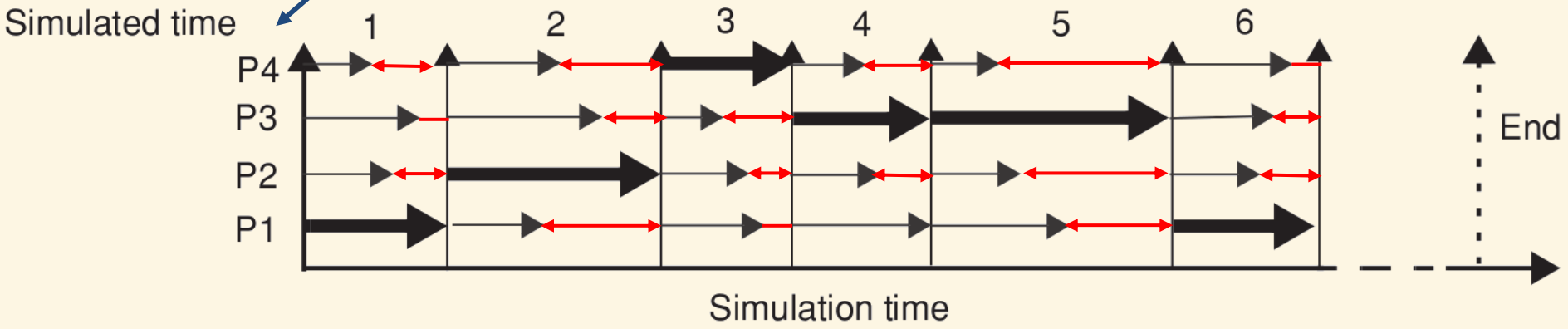
Is it really this bad? What assumption was made here?

Disadvantage

Under utilisation of the host platform if threads are idle for synchronisation

Discrete-Event Simulation

Every target processor Pn is mapped to a separate host core



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Disadvantage

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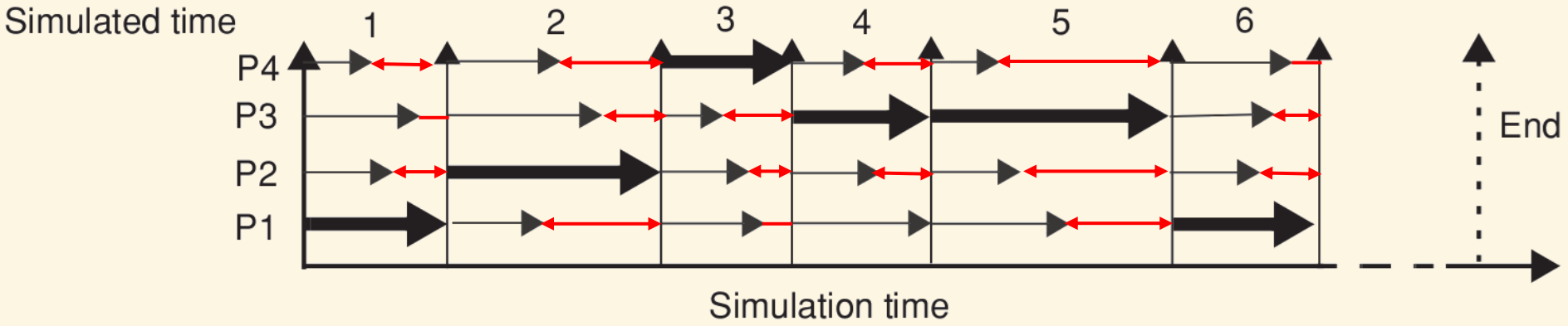
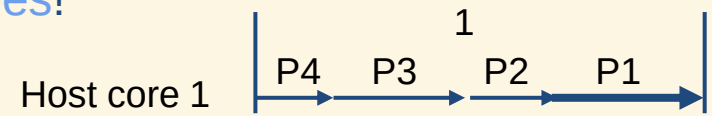
Target vs Host Cores

There is **no relation** between the number of target cores and the number of host cores!!!

Discrete-Event Simulation

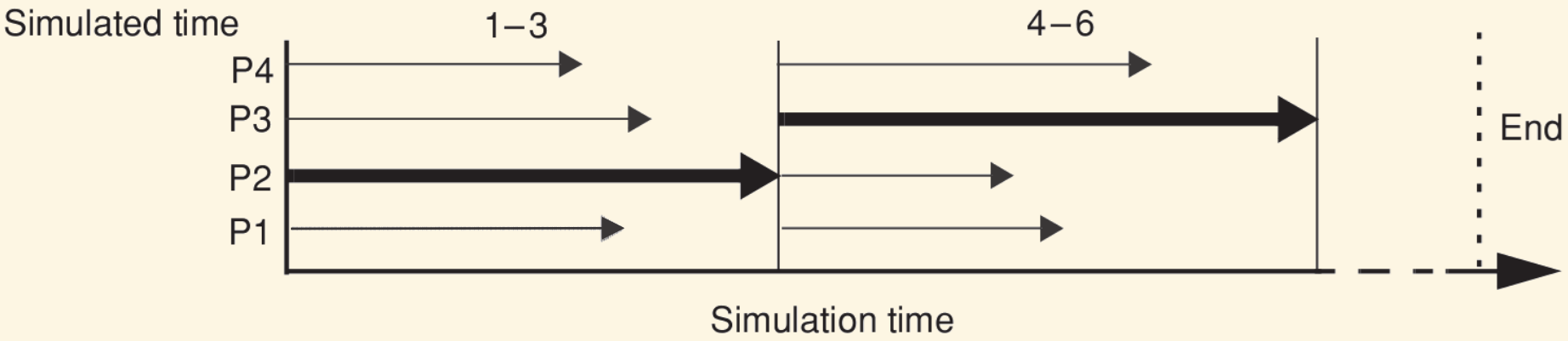


Utilisation of host depends on variation in processing time of a cycle, but also on the amount of host cores!



Quantum Simulation

Synchronize threads at larger time-steps, e.g. 3 cycles



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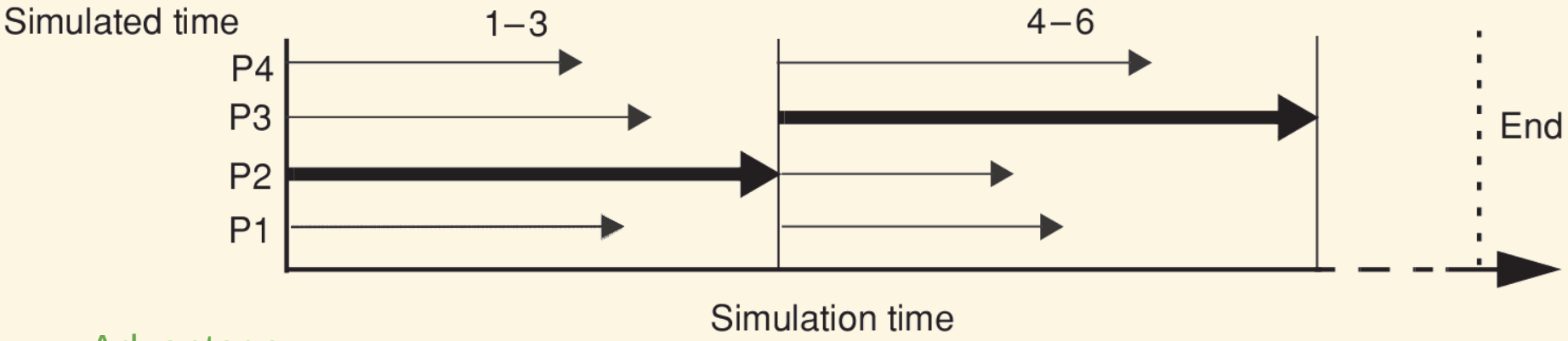


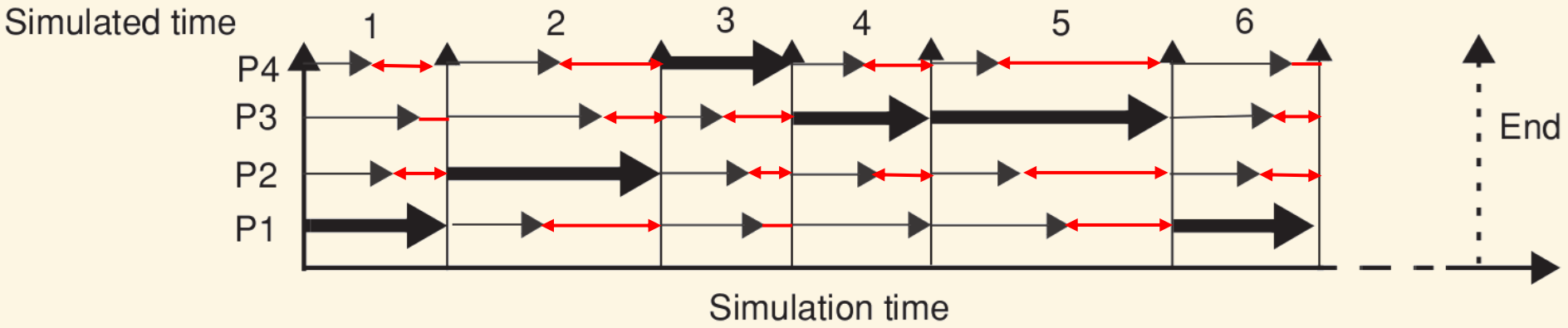
Advantage

Utilisation improves, because the variation of processing is amortized over longer sections of simulation

Disadvantage

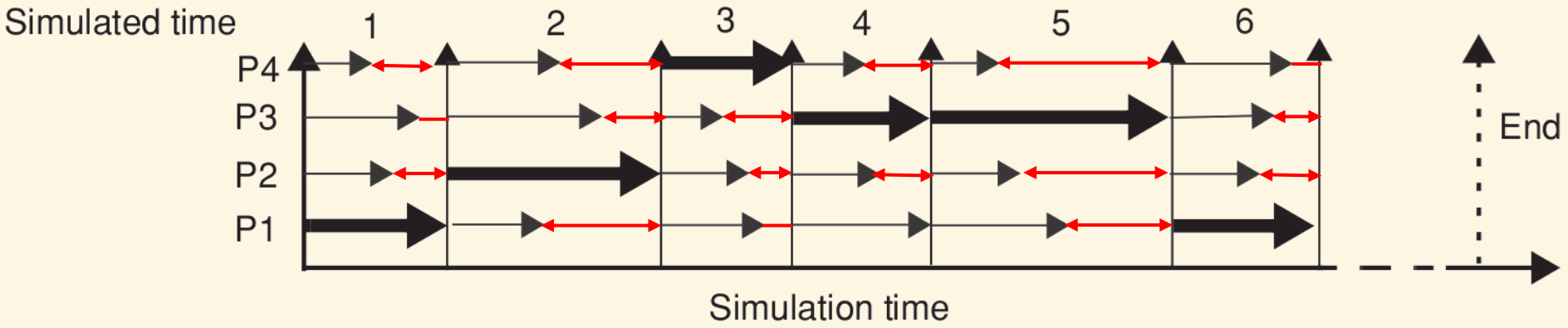
No longer cycle accurate

Slack Simulation



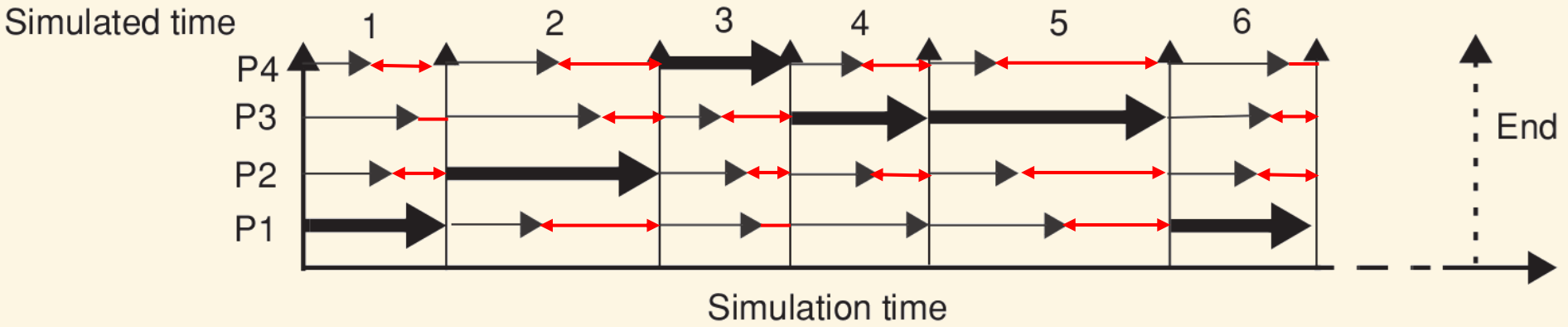
Start with discrete-event simulation schedule

Slack Simulation



Instead of waiting in the red areas, use slack to process ahead

Slack Simulation



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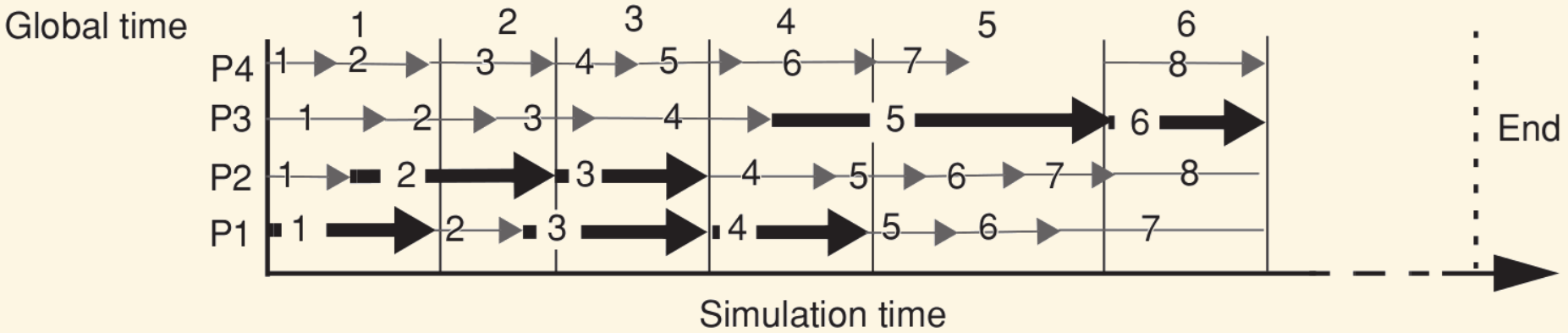


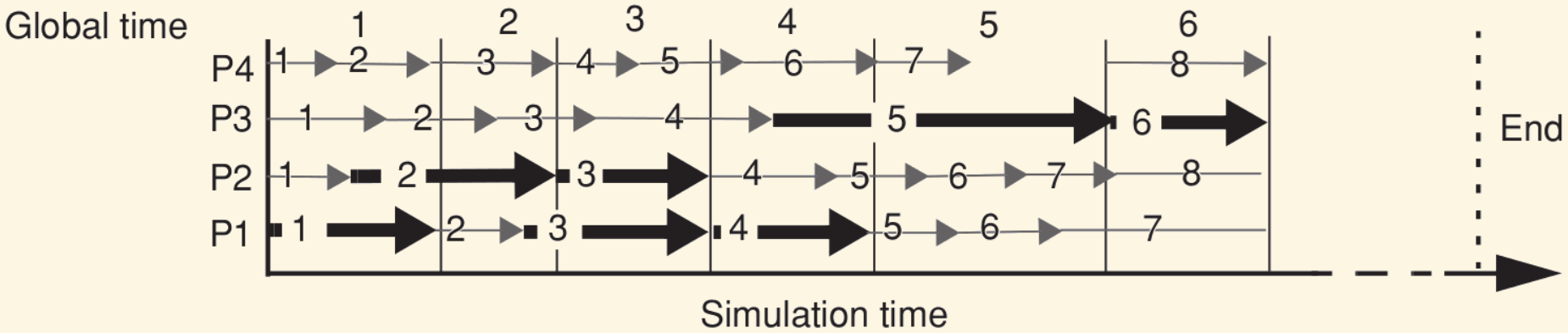
Slack Simulation

Side-effect: Drift

The cores might be simulating different points in time, and could drift apart

Mitigation

Allow a maximum drift (or slack), and synchronize when this value is exceeded



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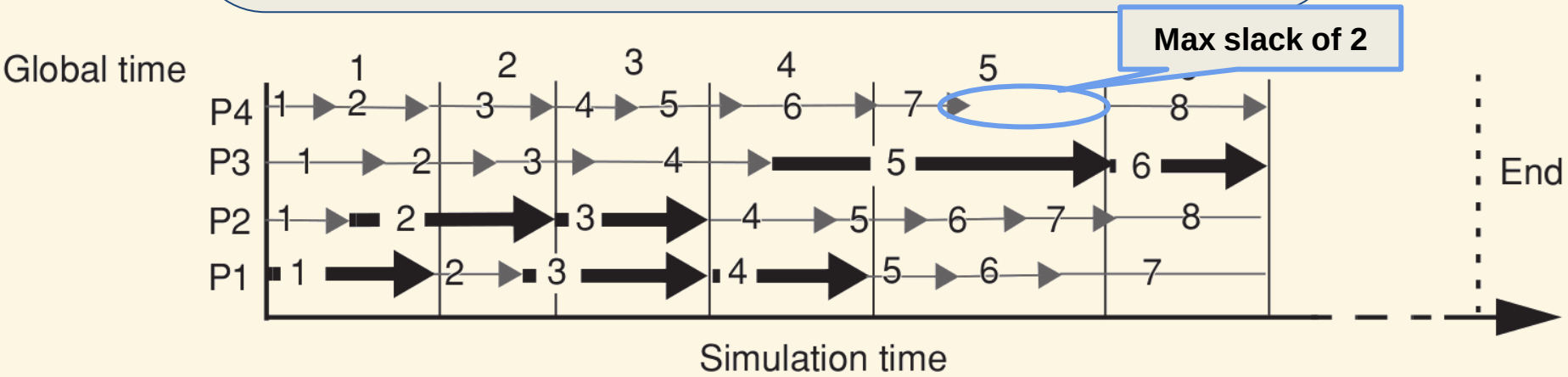
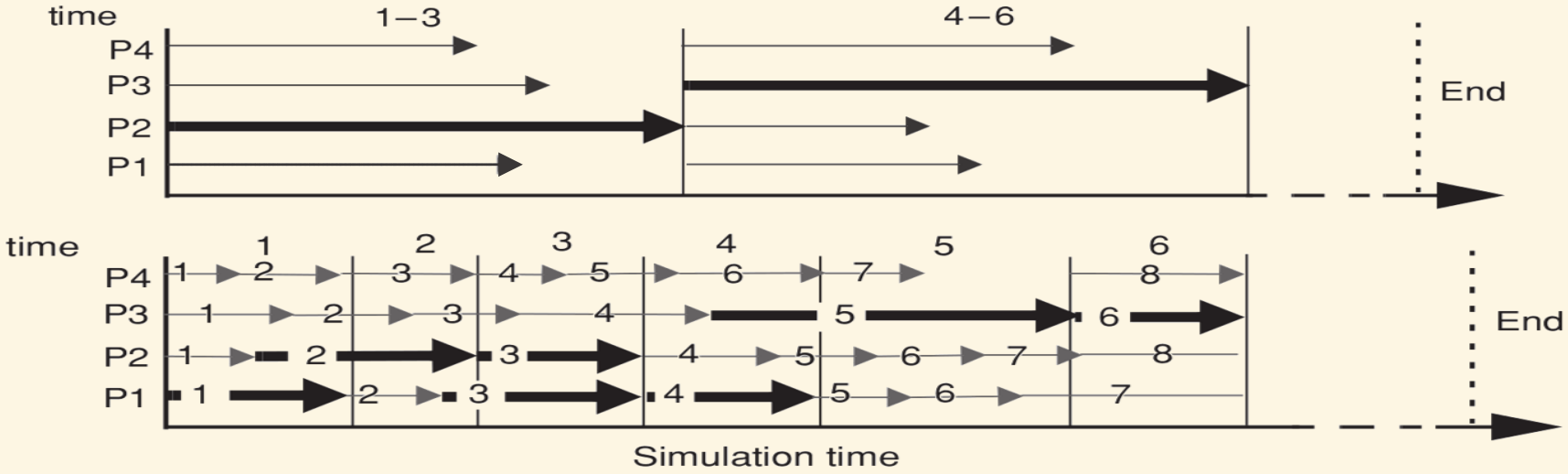


Slack versus Quantum simulation

In quantum simulation, the core simulation times always stay within a cycle window, which is fixed in global time.
Also in slack simulation the simulation times stay within a window, but with the key difference that this is a sliding window.



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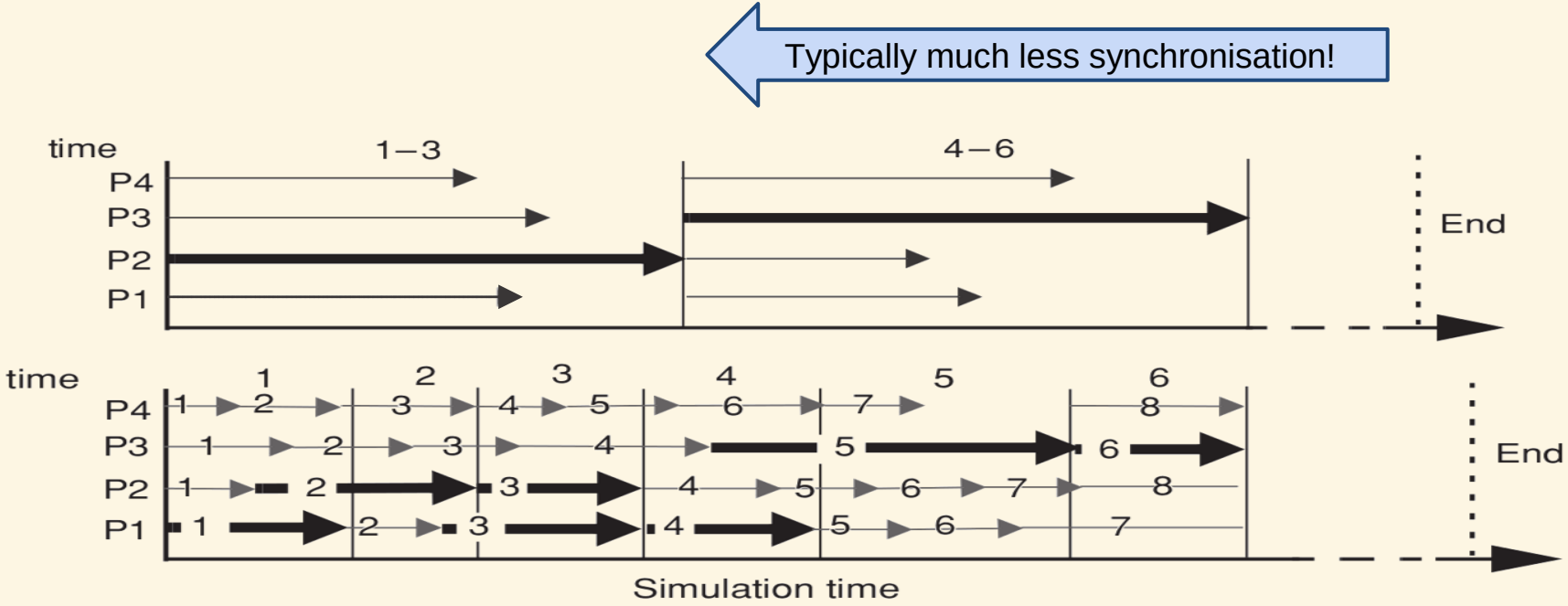

Still not good enough

From the paper ***Graphite: a Distributed Parallel Simulator for Multicores***

"Simulation slowdown is as low as 41× versus native execution"

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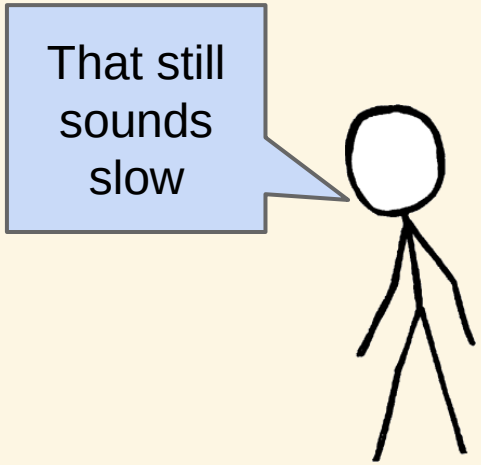

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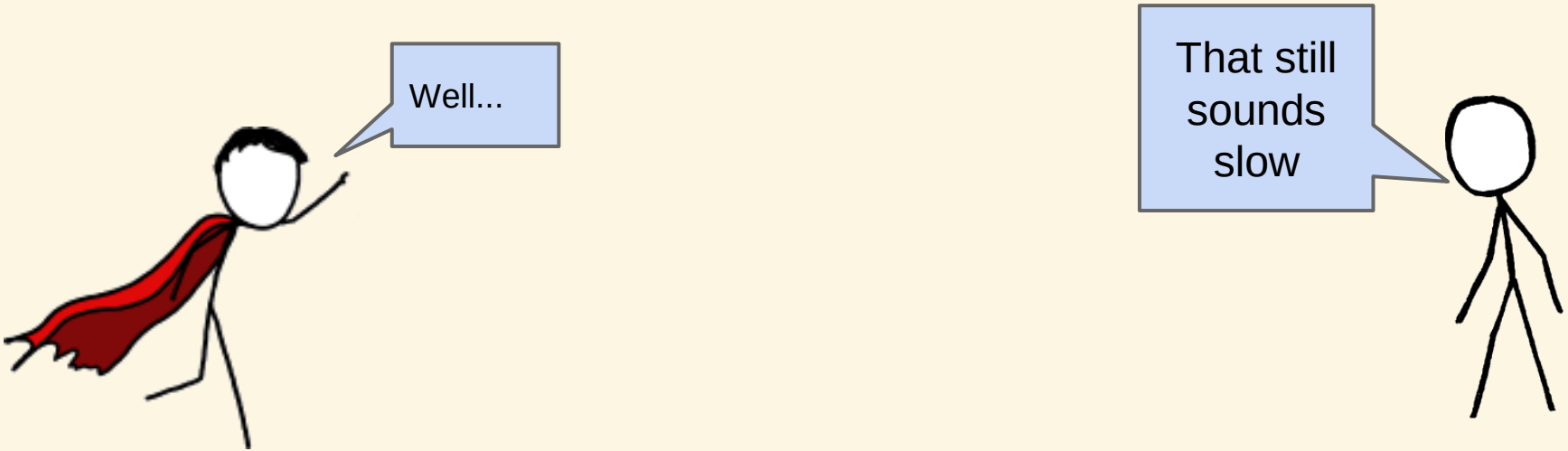

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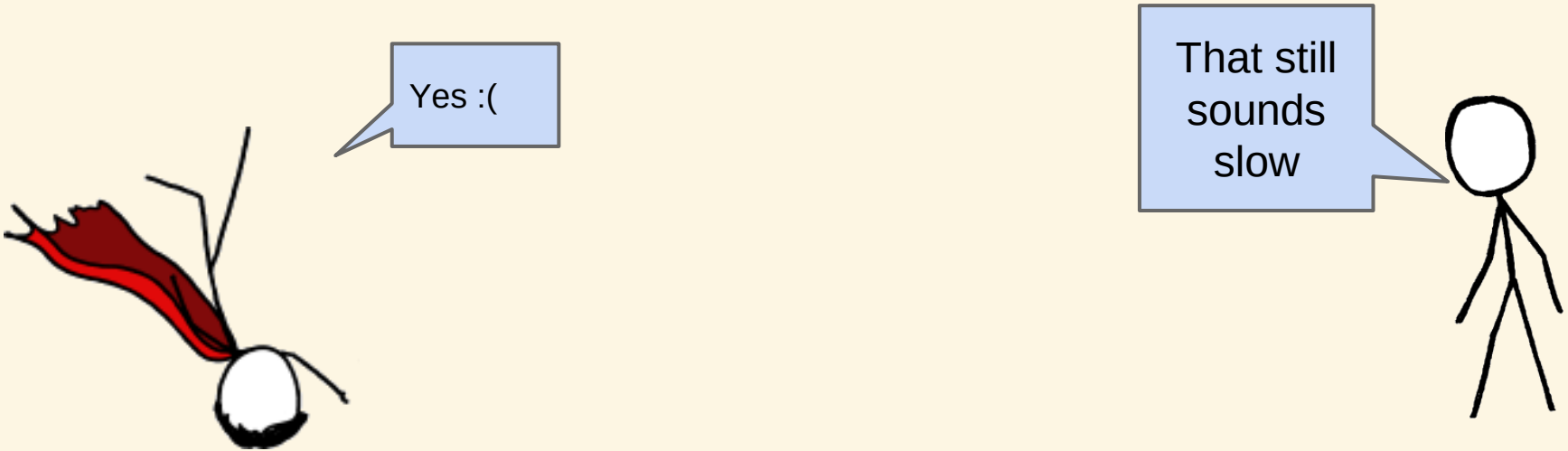

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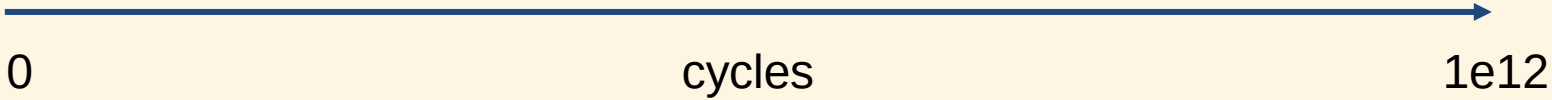
Question

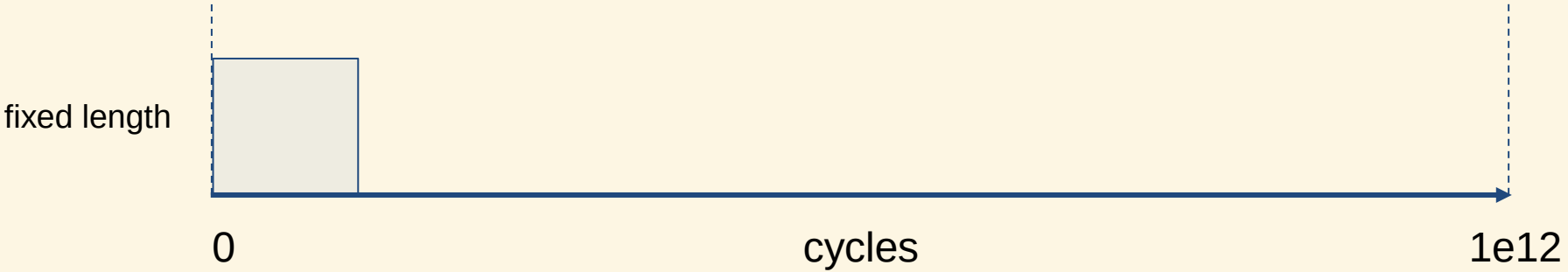
What can we do if it still takes weeks or months to simulate a full benchmark?



Workload Sampling

Naive Approach

Only simulate first X cycles



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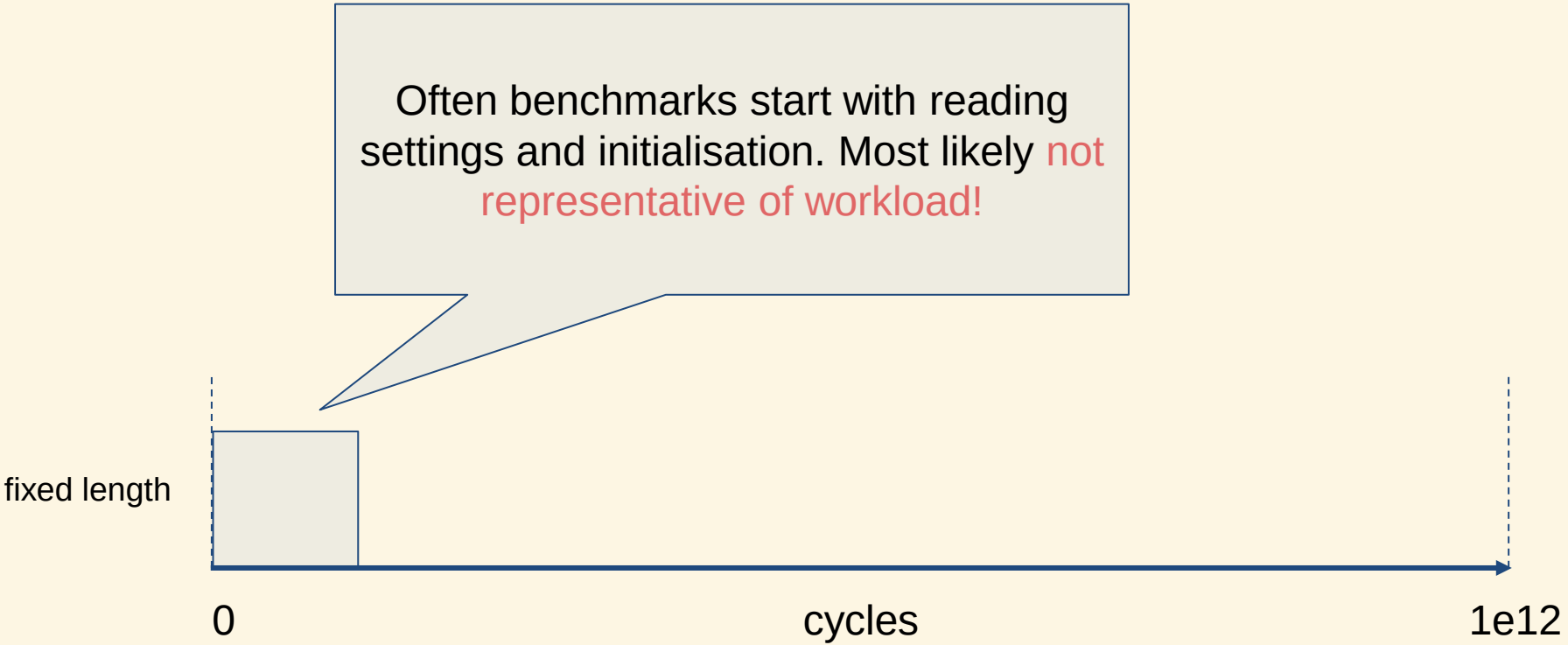

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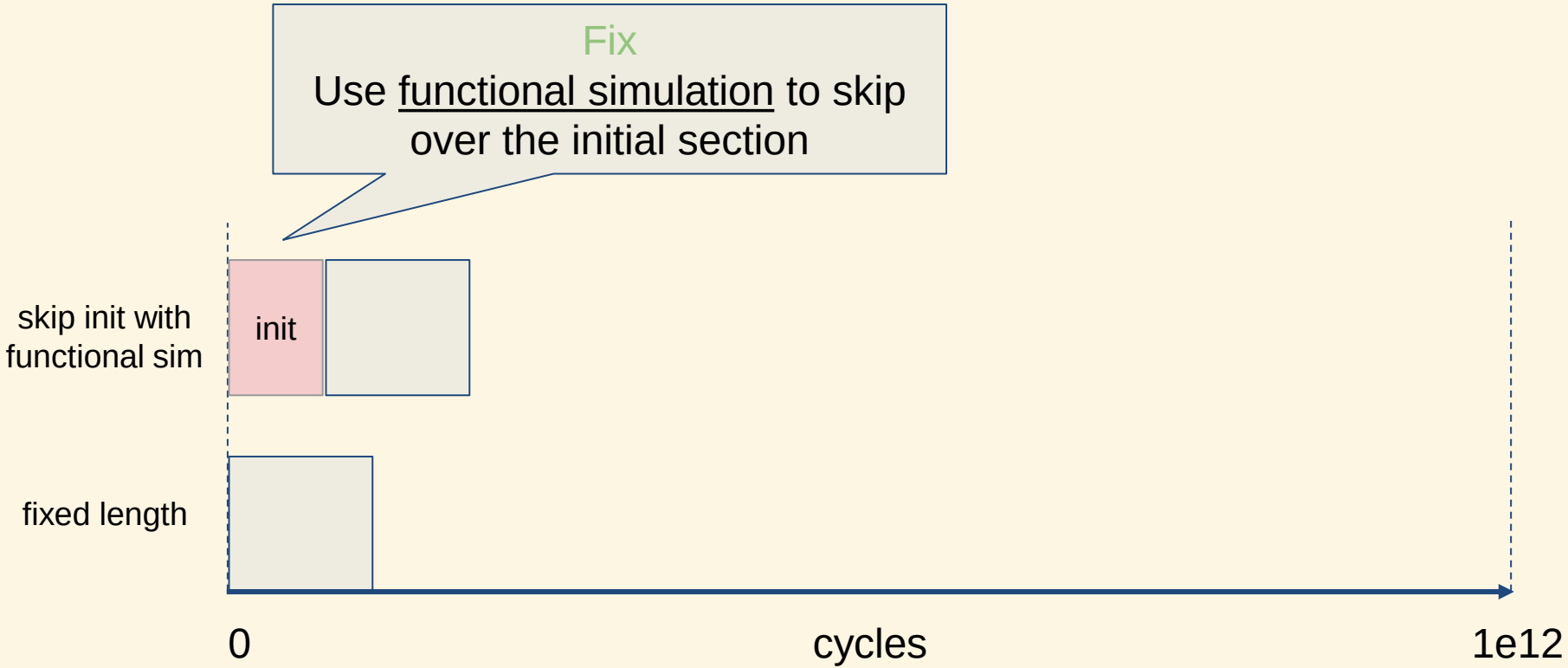
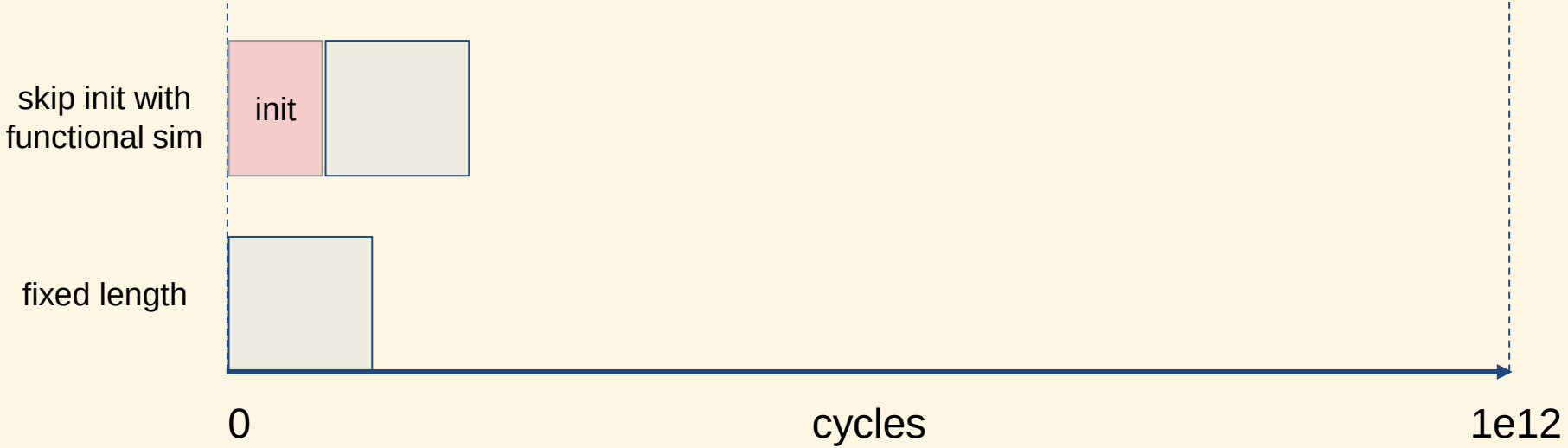


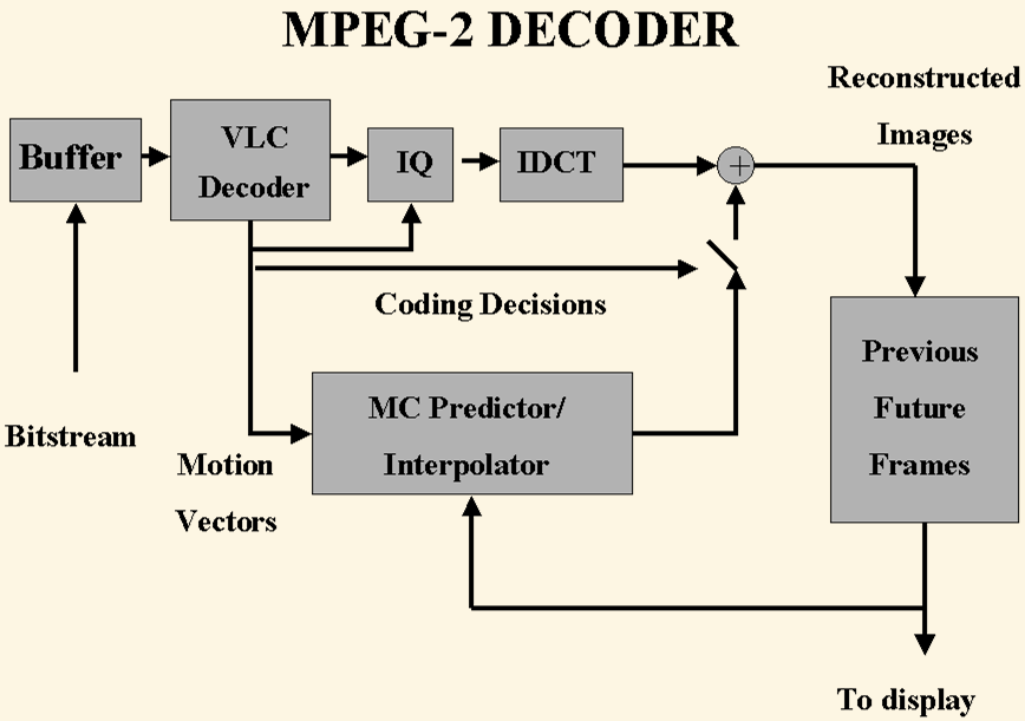
Workload Sampling

Question

Is the window always a good representation of the benchmark? Why/why not?



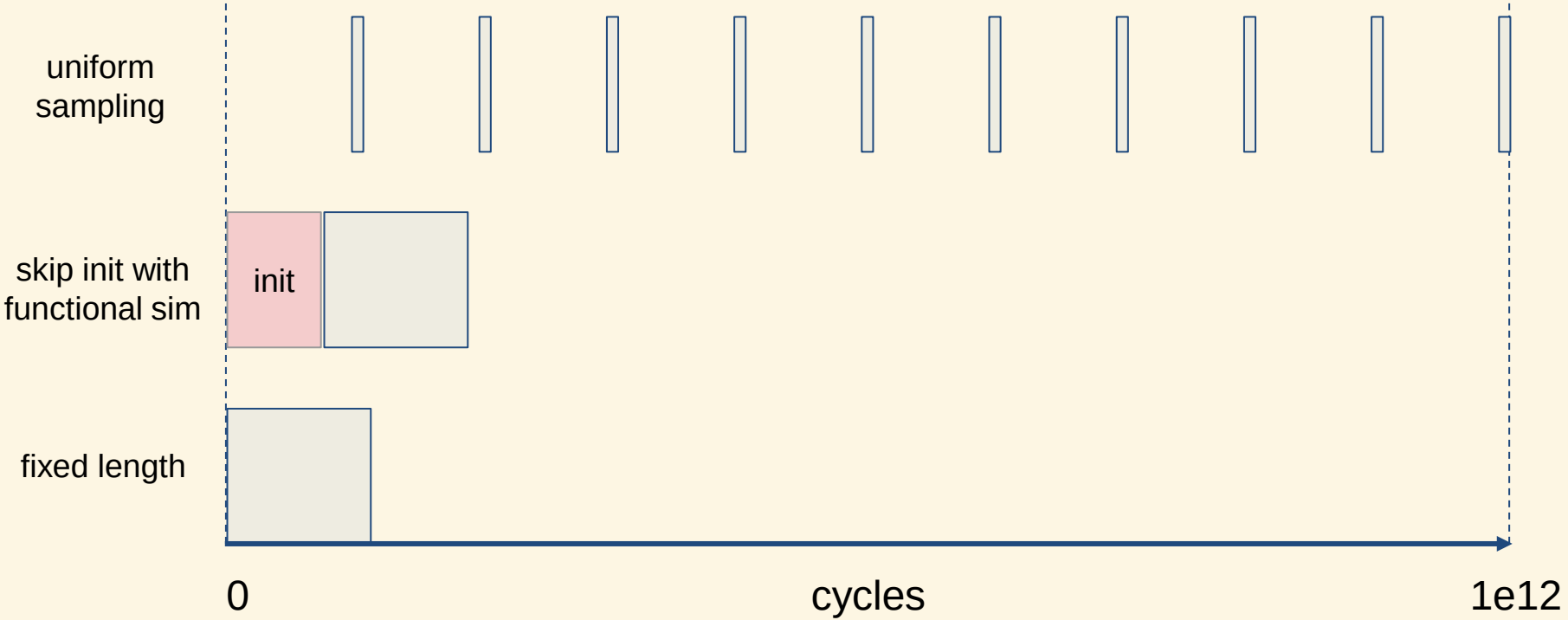
Program Modes



Real world programs spend time in different modes, which can have very different characteristics

Workload Sampling

Sample uniformly over the program, hopefully capturing the dominant modes



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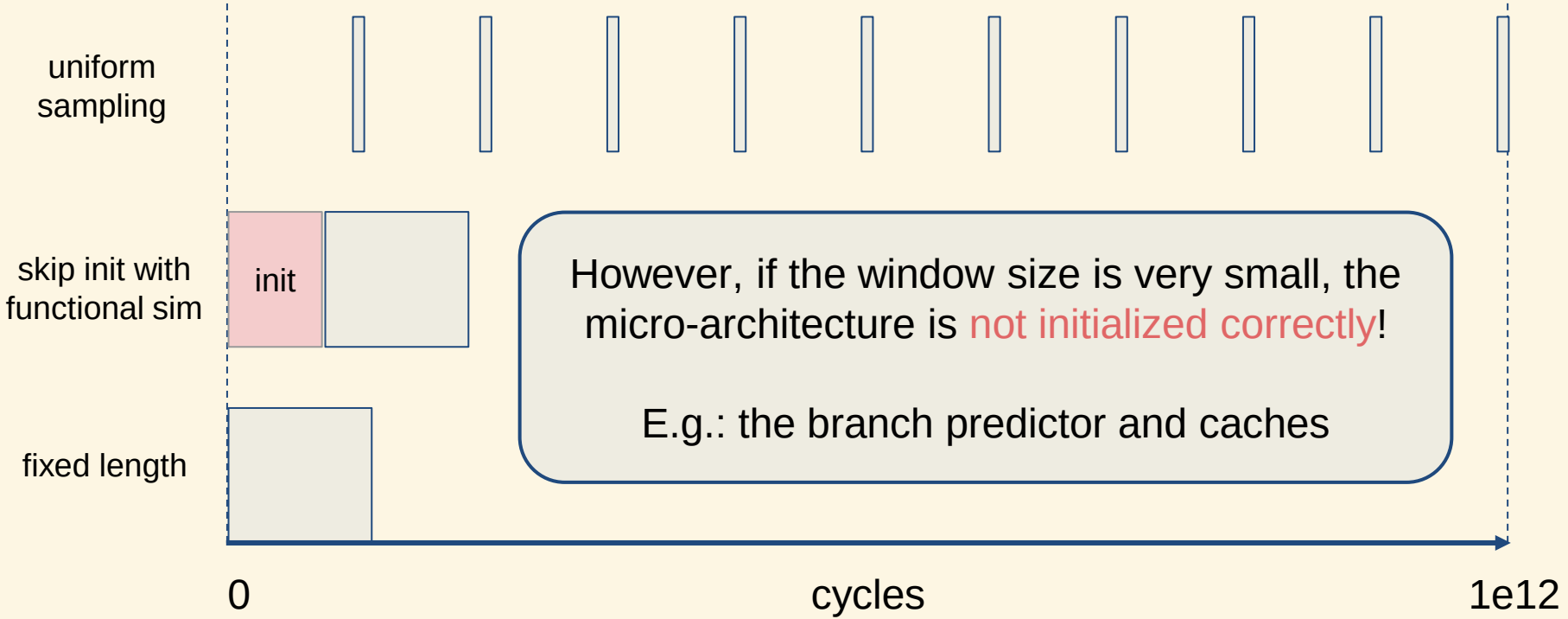
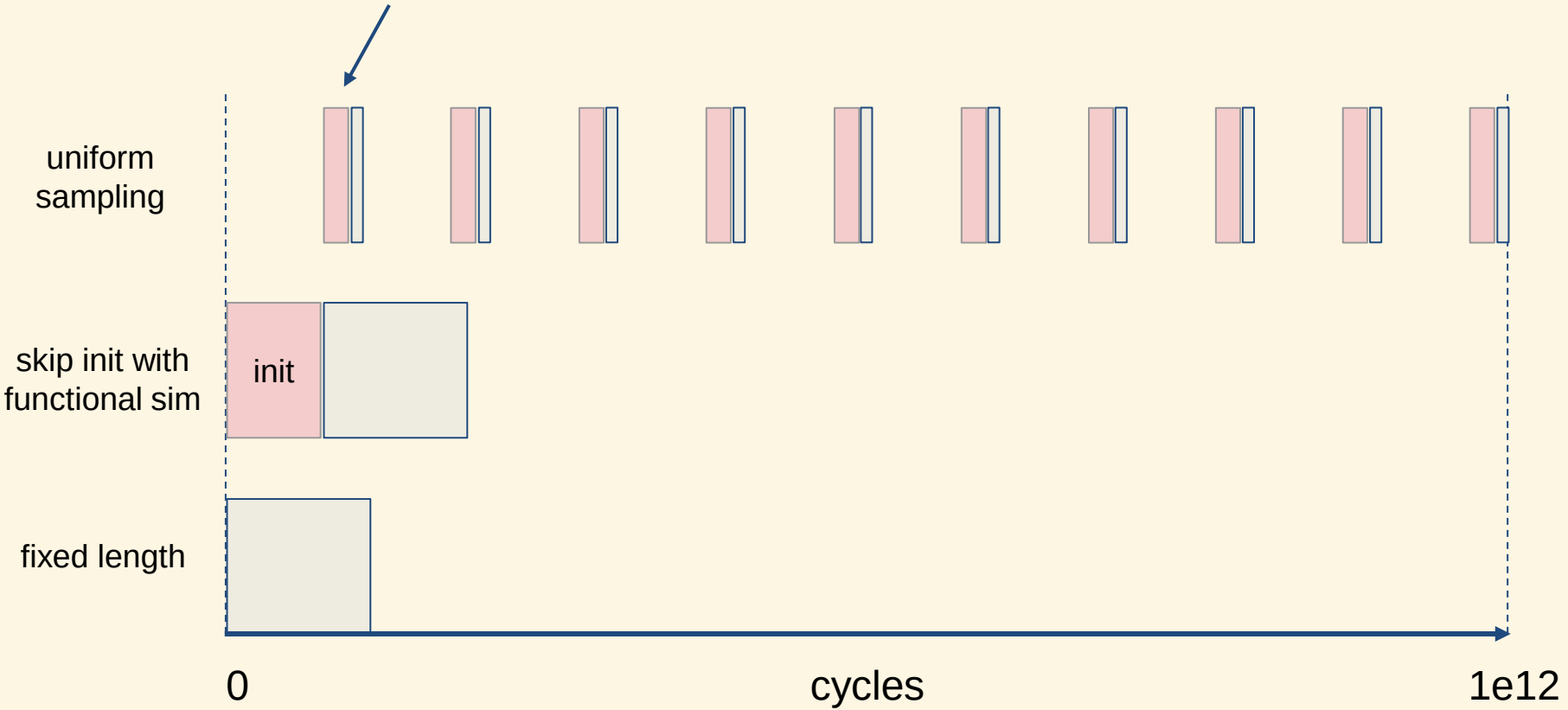


Workload Sampling

Solution: add warm up period before every window



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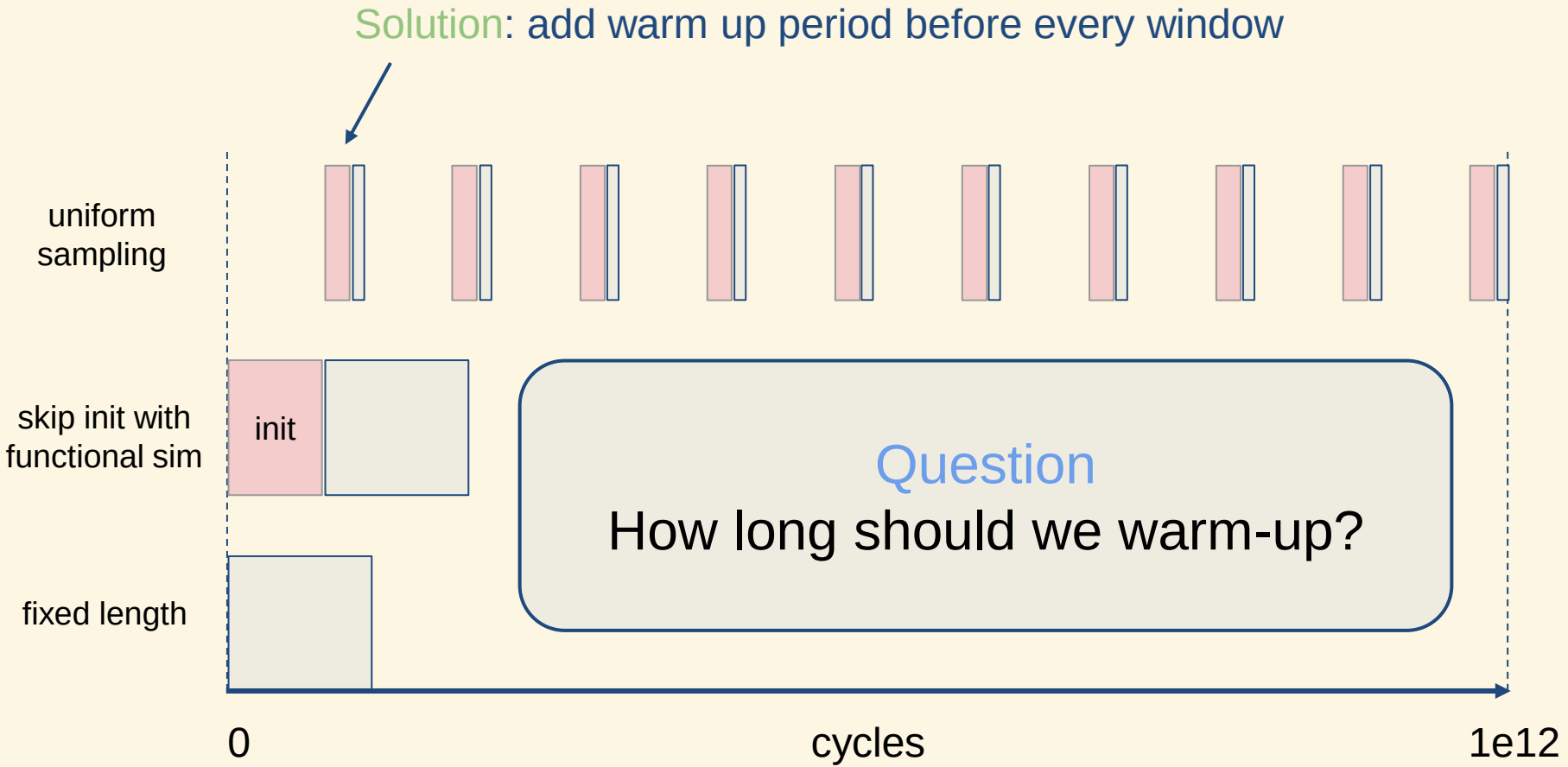

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[1] *SMARTS: accelerating microarchitecture simulation via rigorous statistical sampling* - Roland E. Wunderlich et al.

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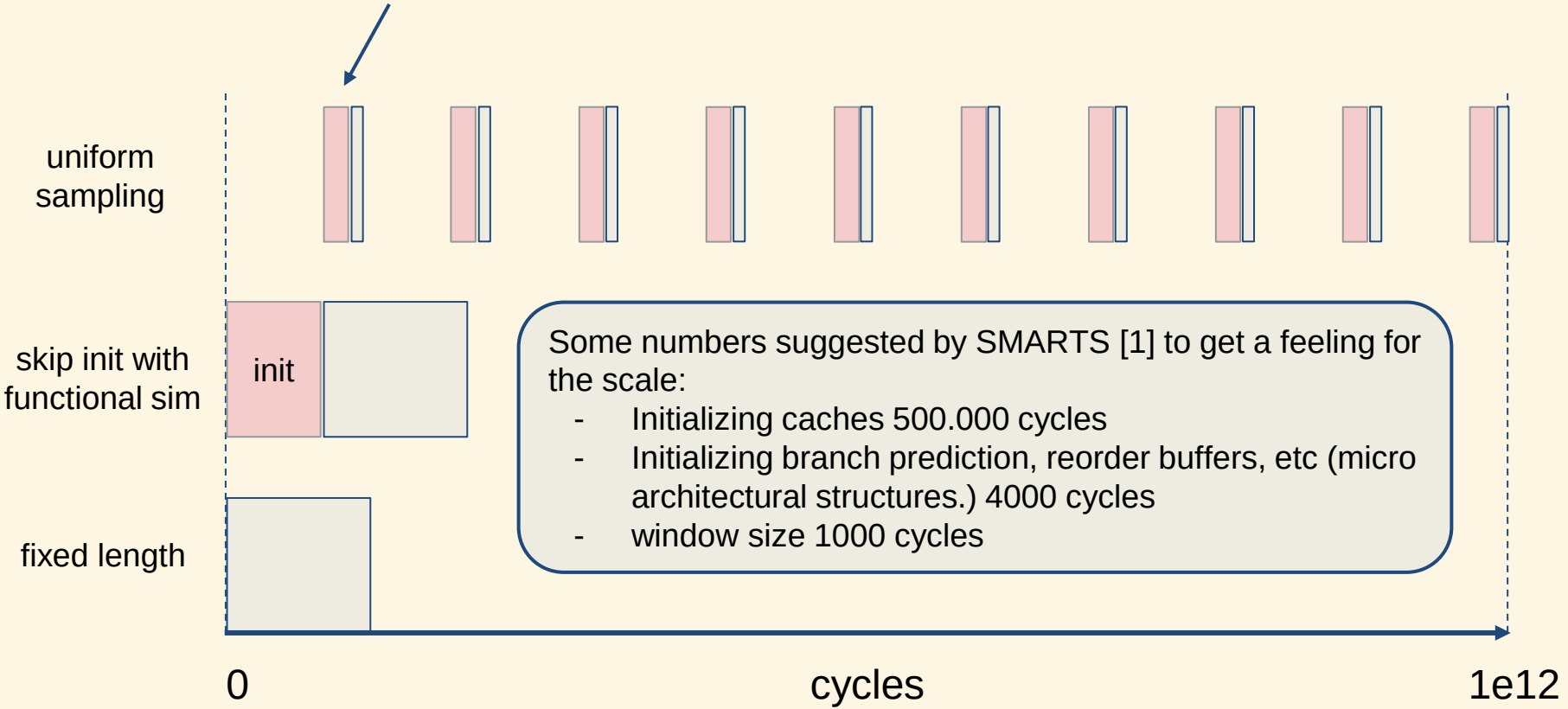

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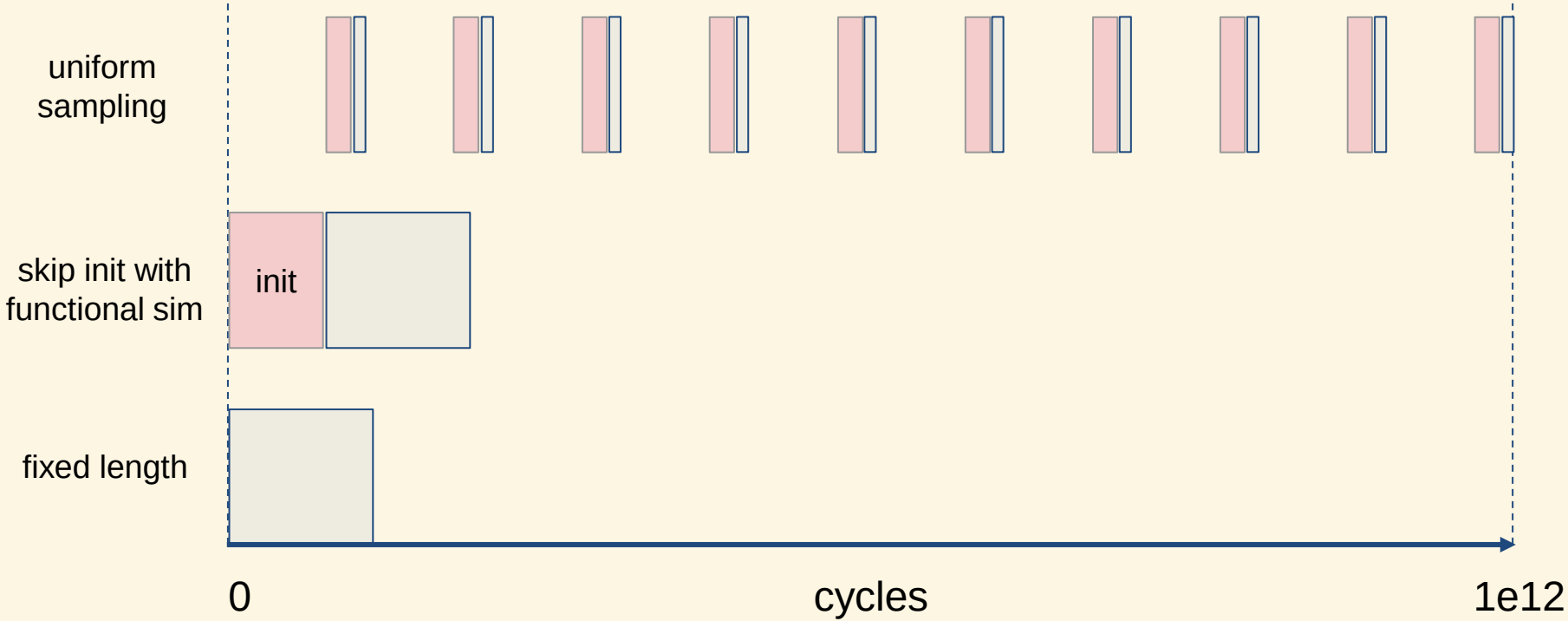

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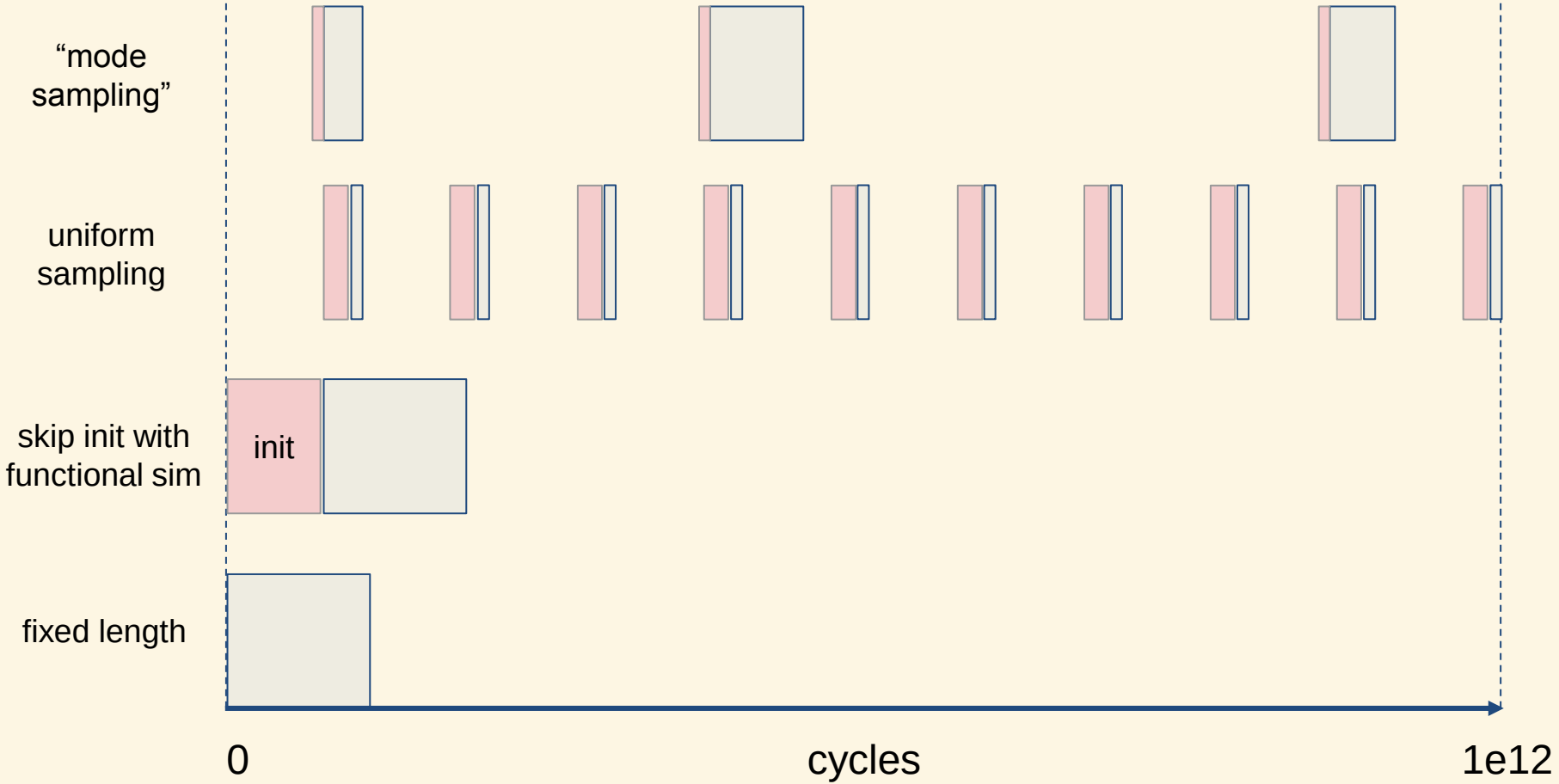

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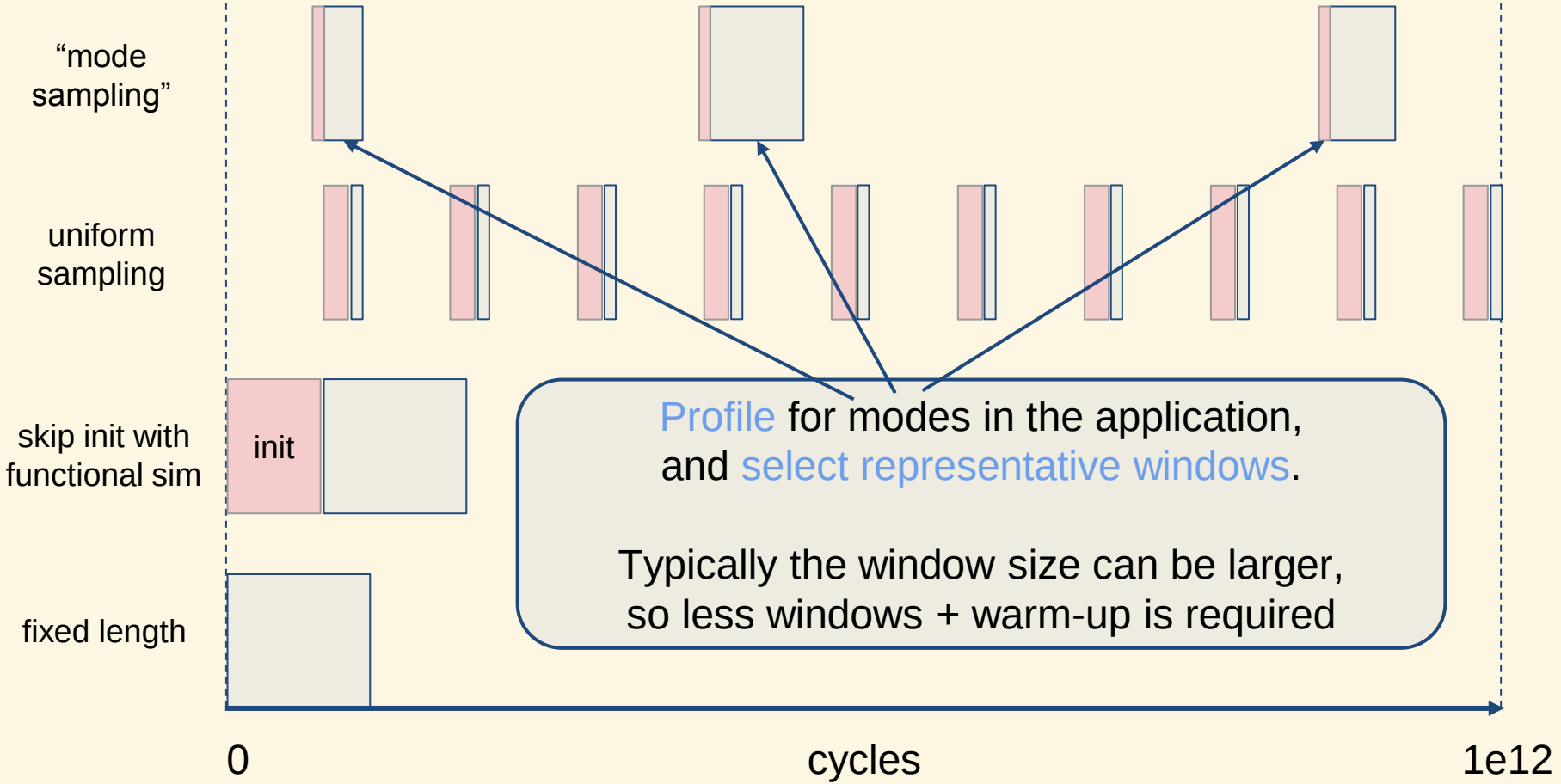

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  - More accurate than models
  - Cheaper than building hardware
- Simulation detail
  - Full-System vs User-level
  - Functional vs Cycle Accurate (micro-arch.) vs Gate-Level
  - Execution- vs Trace-driven
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You can find more (optional) background information in chapter 9 of the book by Dubois et al.